

MS-16J3/MS-1793

Shark Bay Mobile

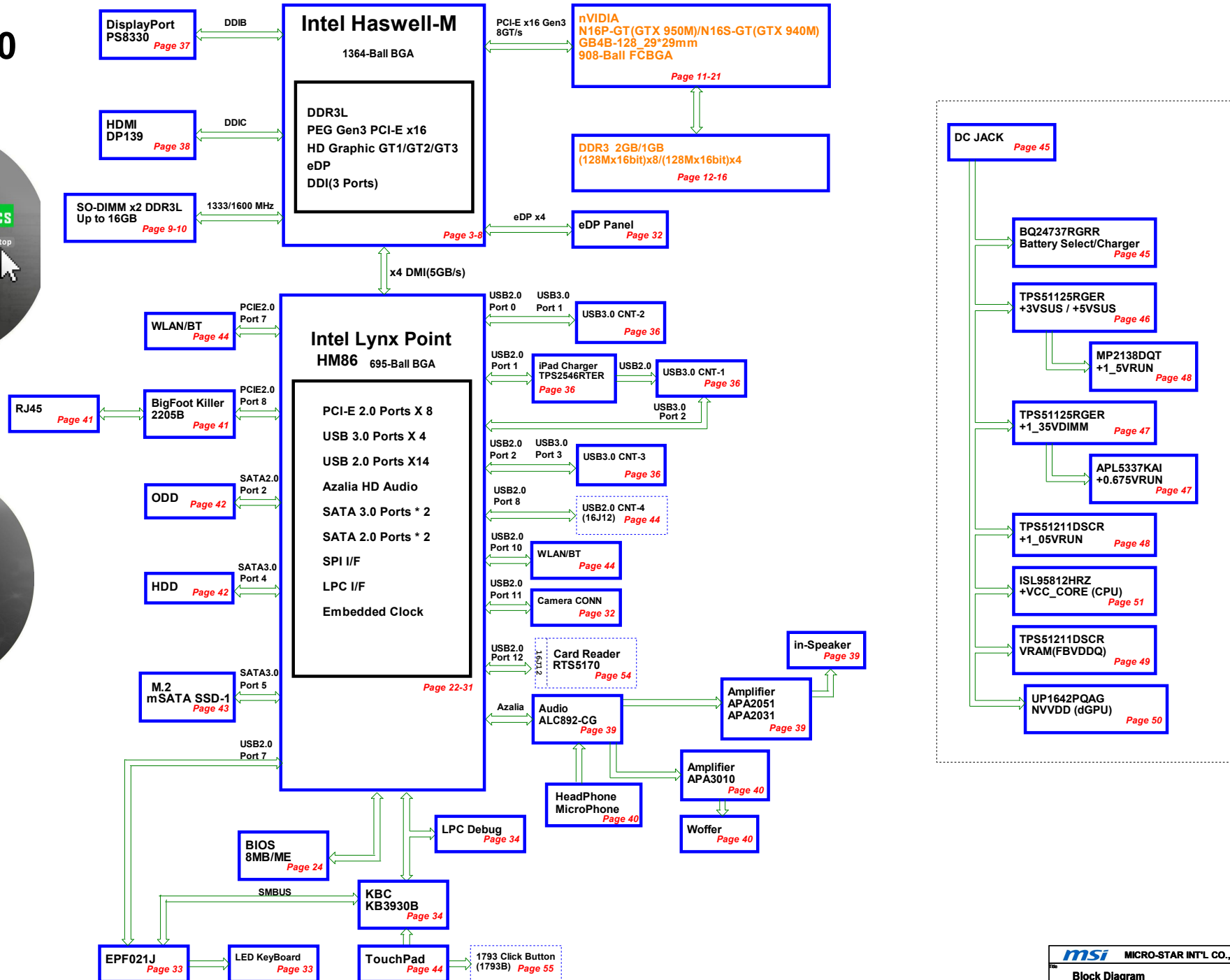
Ver:1.0

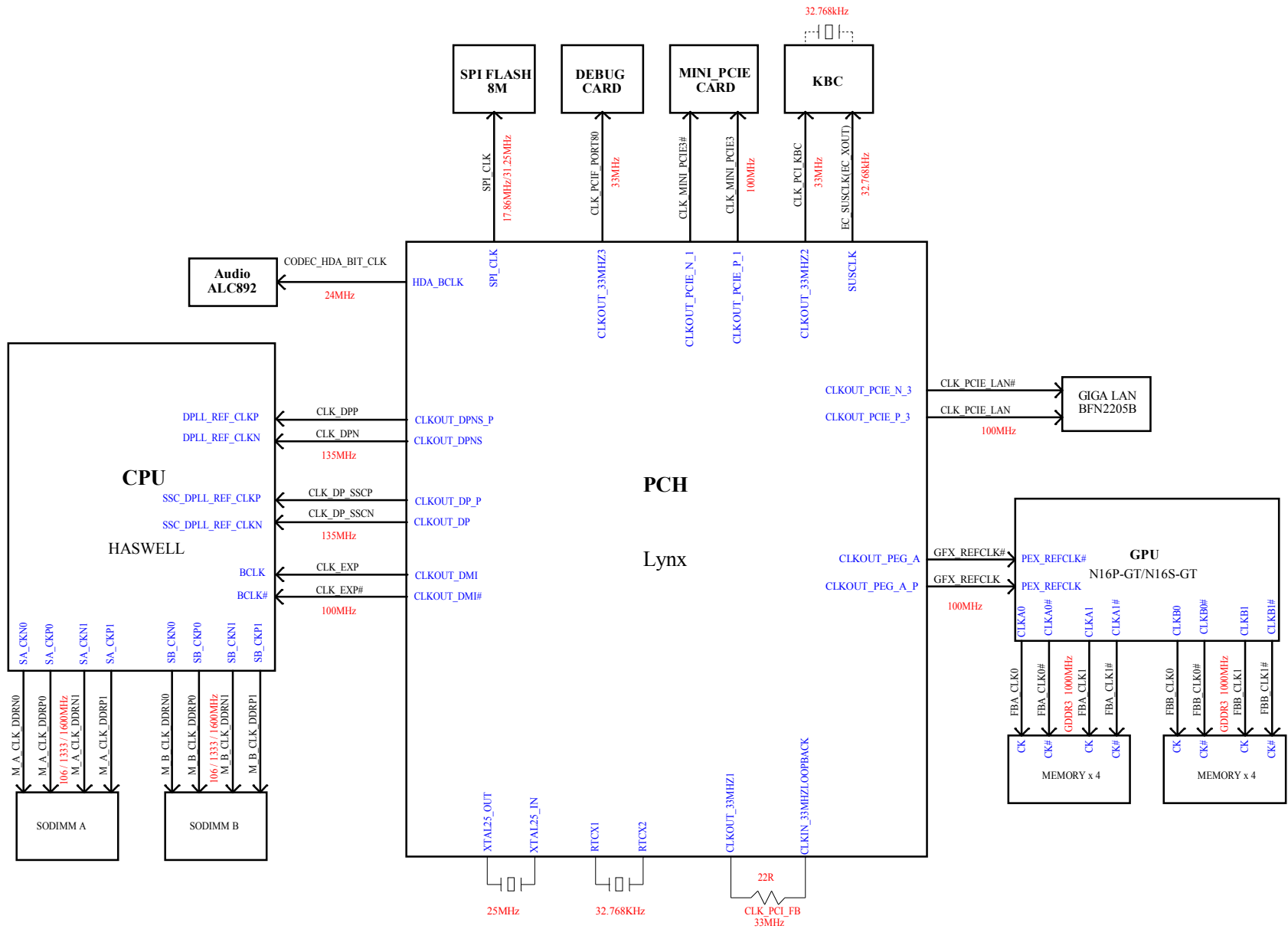
Laptop Schematics

www.Telegram.me/schematics_laptop

BIOS Archive

www.Telegram.me/biosarchive





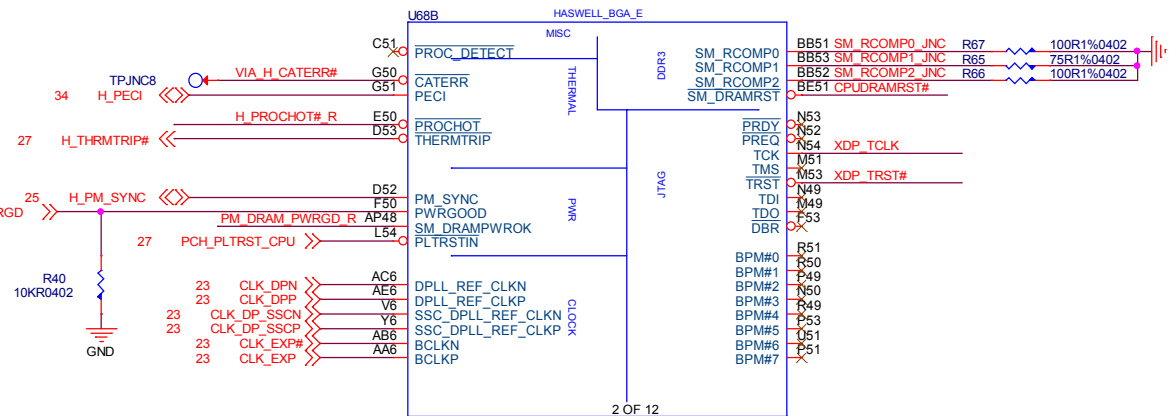
Haswell (DMI,PEG,FDI)

```
PEG RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils
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Haswell (CLK,MISC,JTAG)

i7-4710HQ, (SR1PX) , 2.5GHz

SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil



I7 4720	HSW
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I7_4720

I7_4720

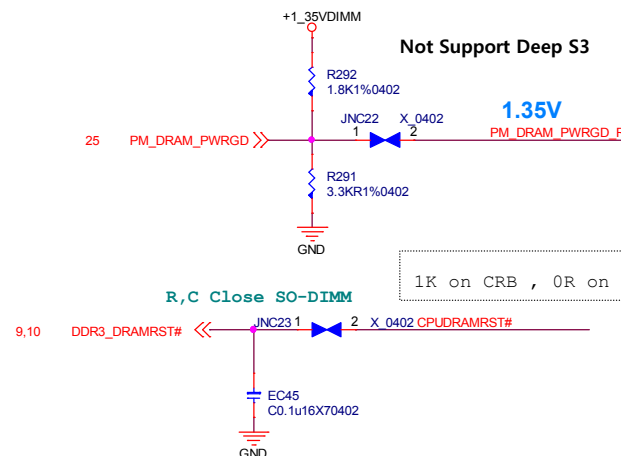
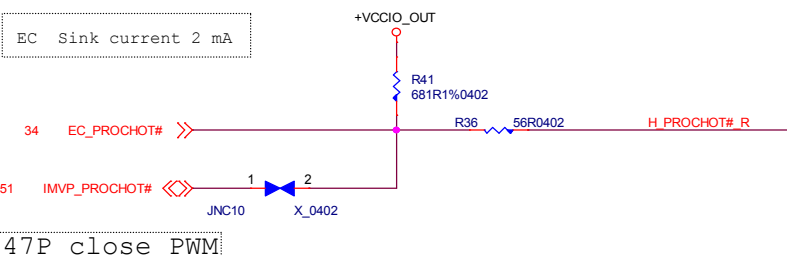
A13-2620135-100

I7 5700	BDW
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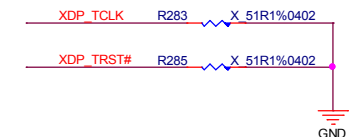
I7_5700



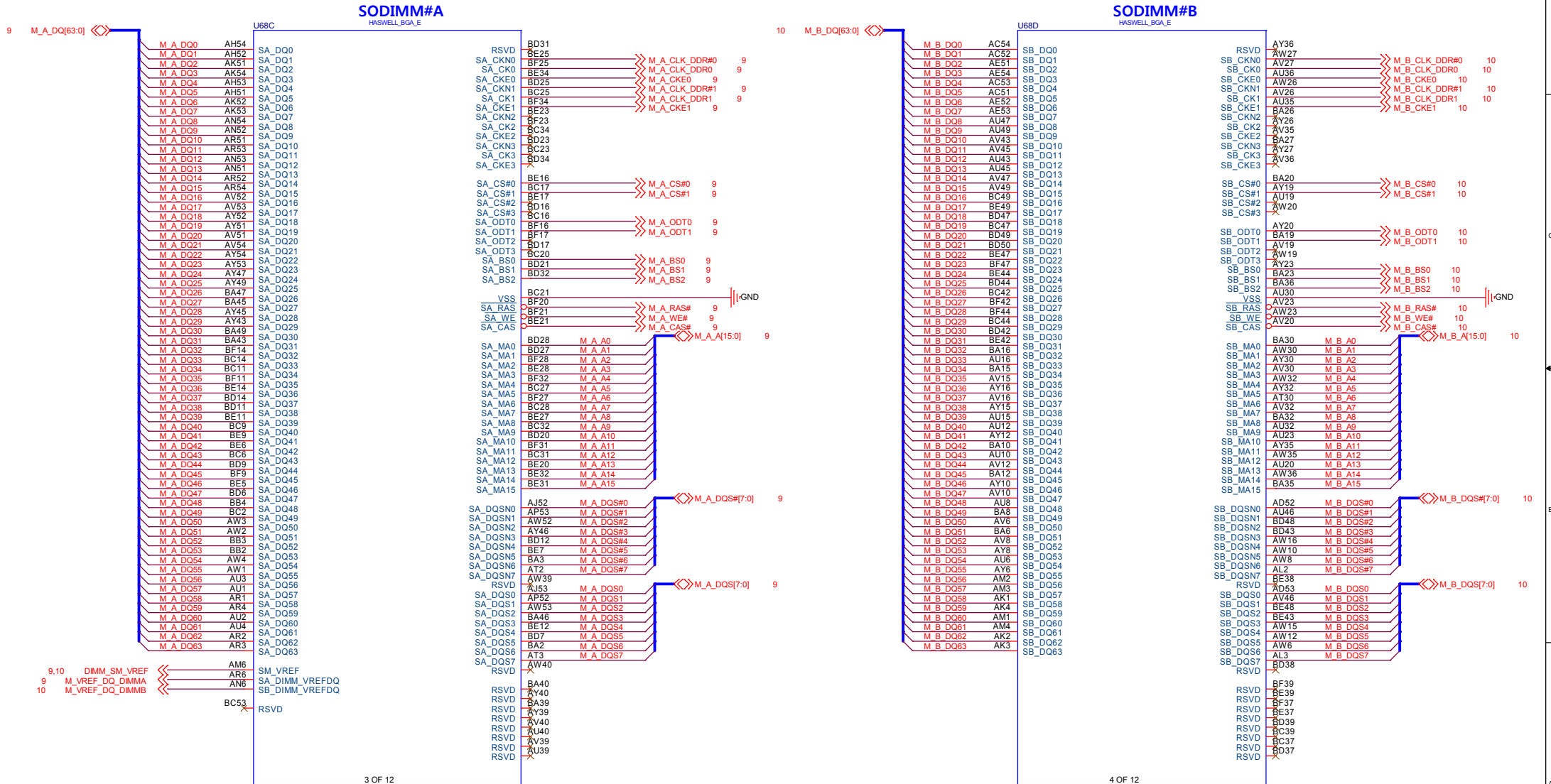
I7_5700
OAD-1812002

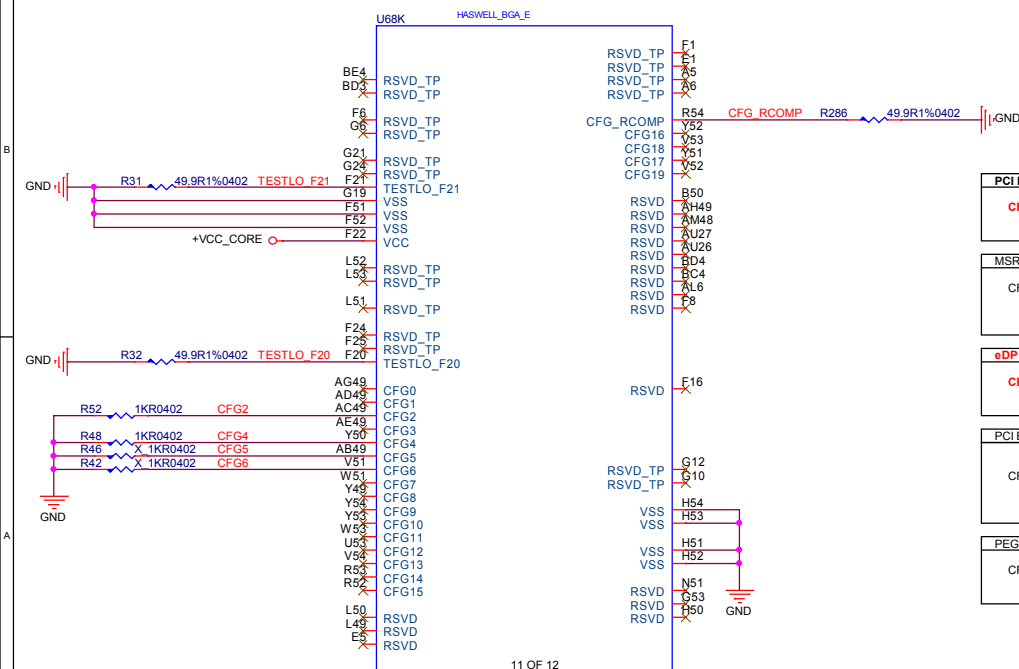
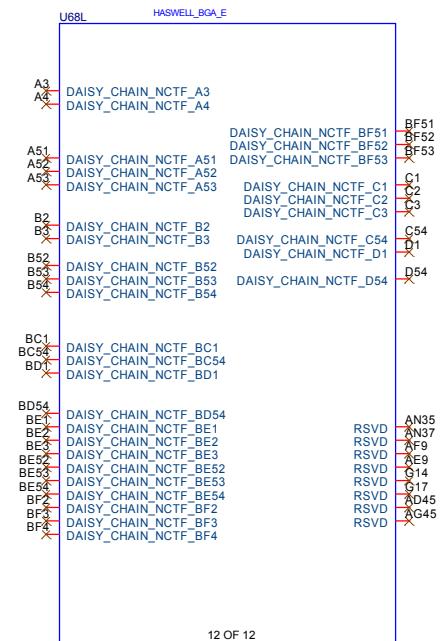
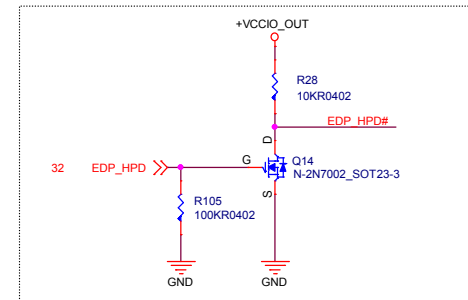
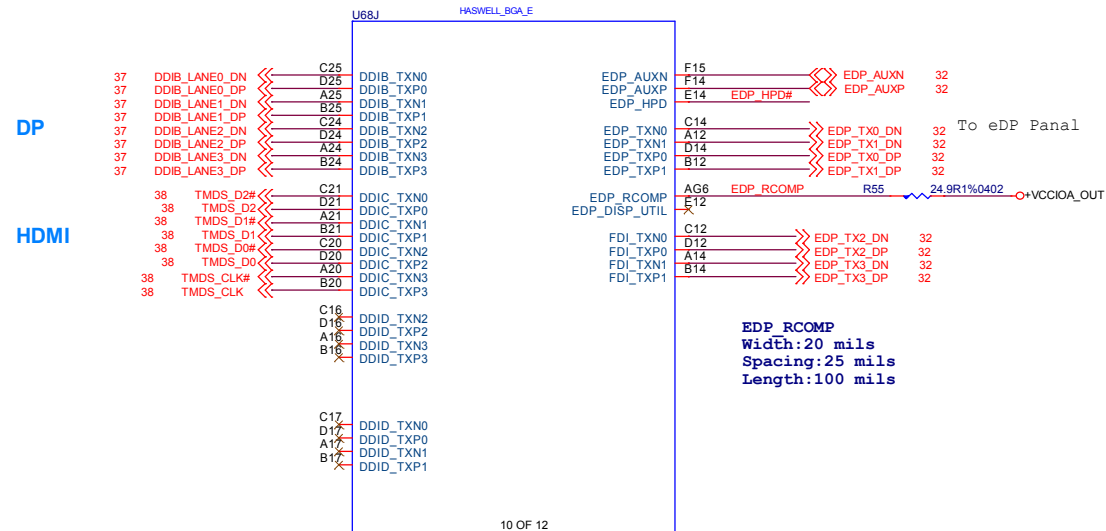


p.11 479493_479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals,
PREQ# and PRDY# signals have adequate
internal bias resistances to support the removal of the
external pull up and pull down on the board
when debug is no longer needed.



Haswell (DDR3L)



Display/Reserved

PCI Express* Static x16 Lane Numbering Reversal	
CFG2	<p>1 = Normal operation</p> <p>0 = Lane numbers reversed.</p>

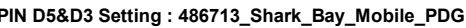
MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden


eDP enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

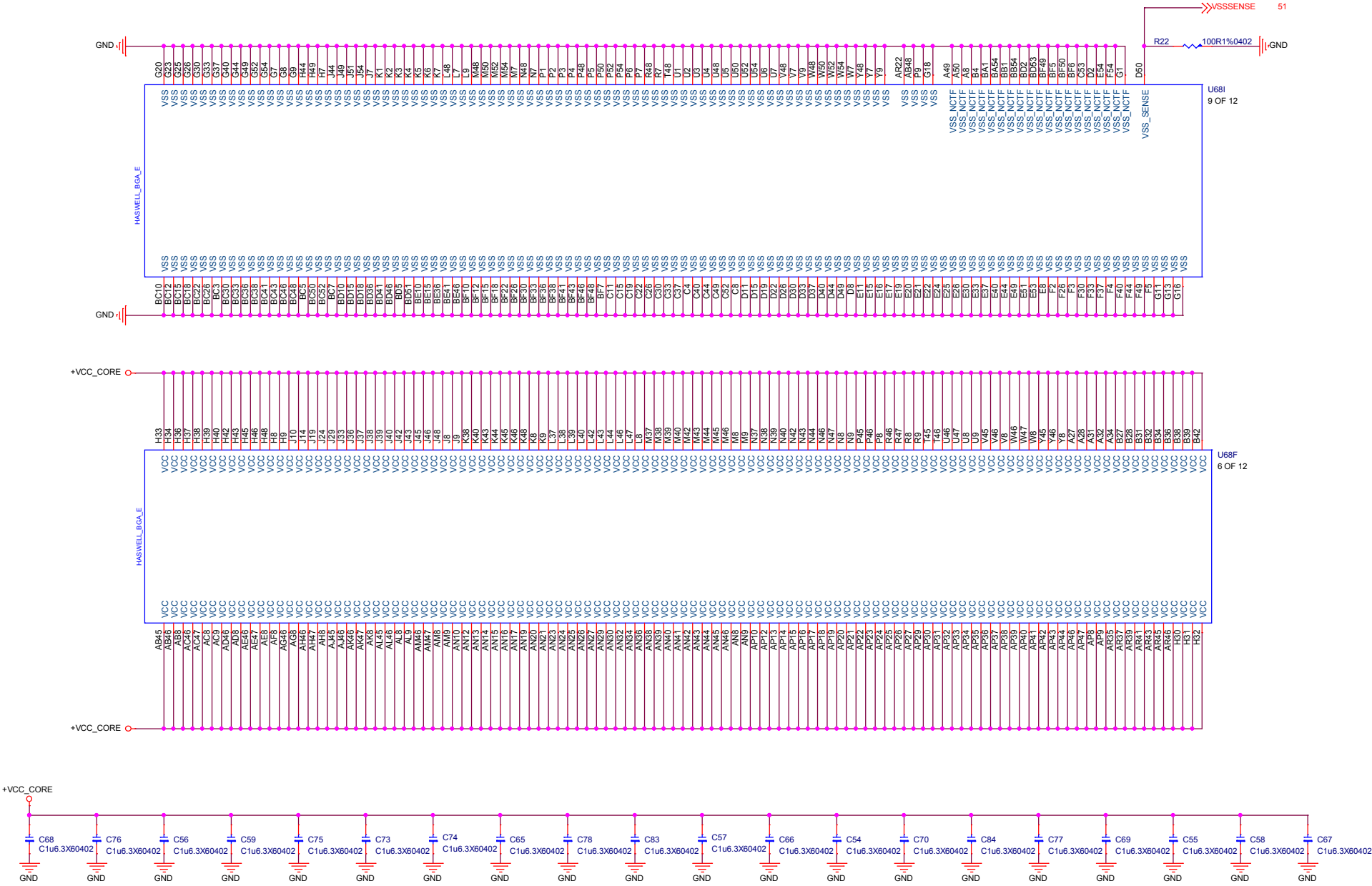
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

U68E

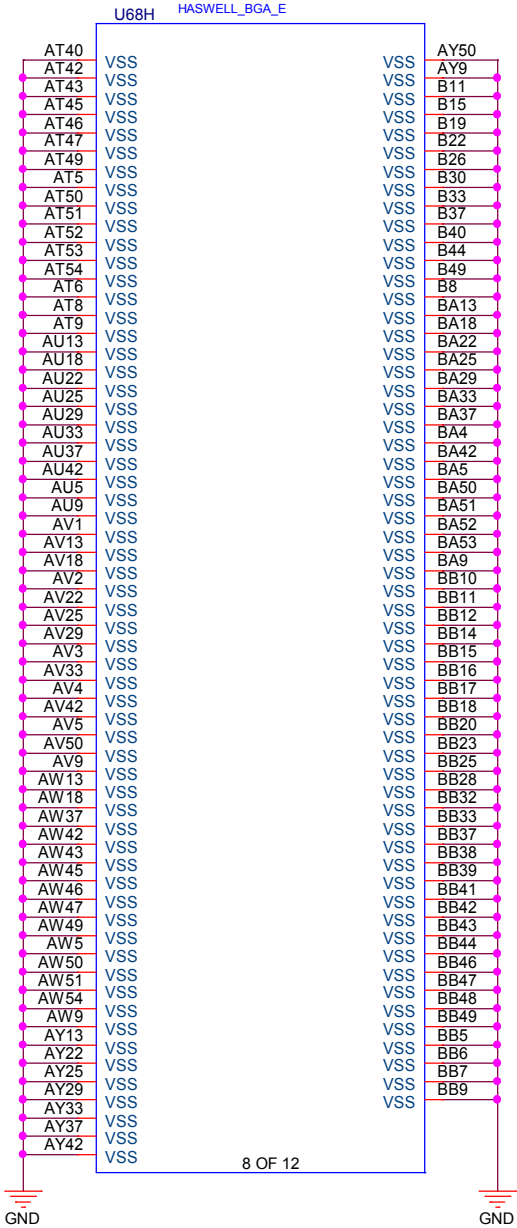
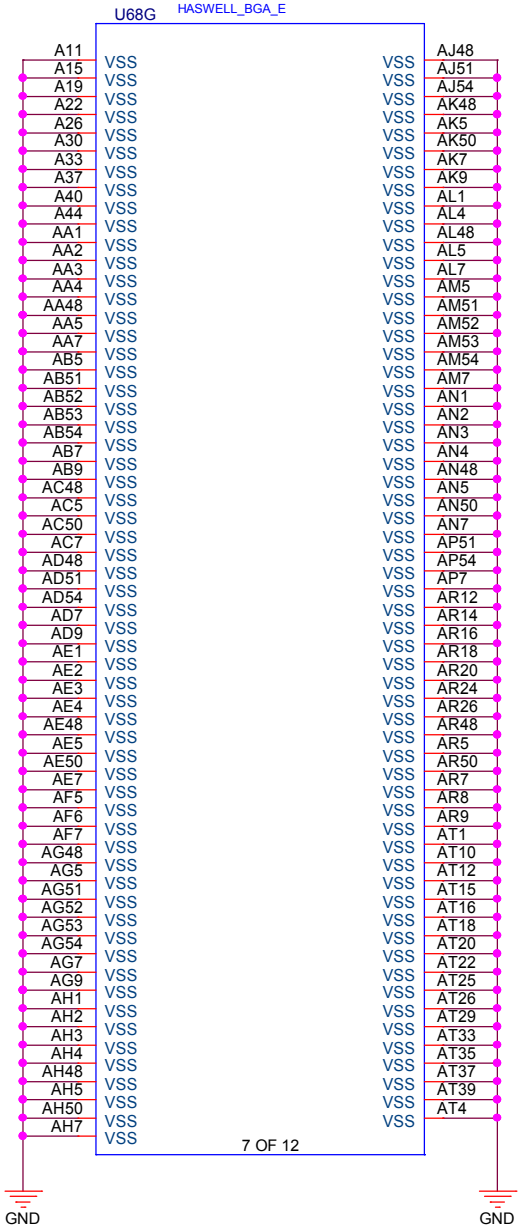


 MICRO-STAR INT'L CO.,LTD.	
Title	
CPU-4 (Power)	
Size	Document Number MS-16J3
Date:	Tuesday, April 14, 2015
Sheet	6 of 60
Rev	1.0

Haswell (Power & GND)



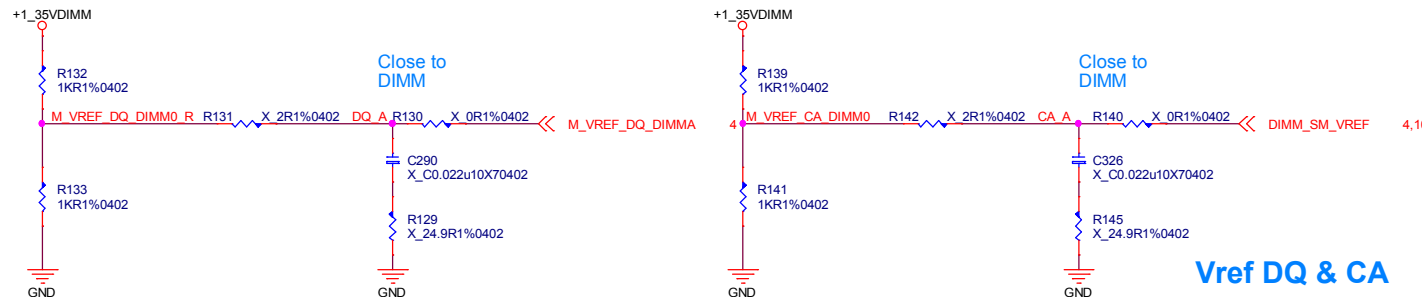
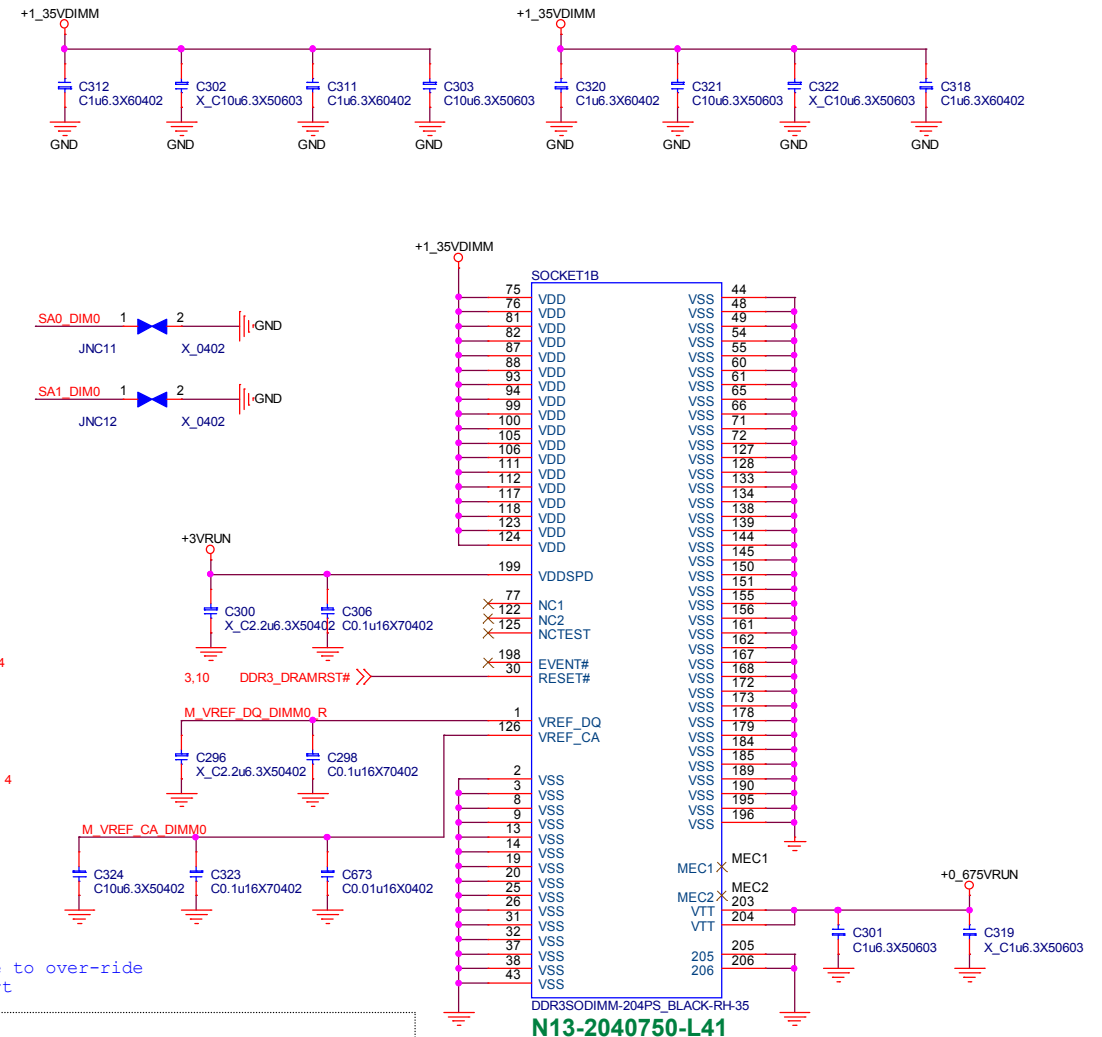
Haswell (GND)



SODIMM#A

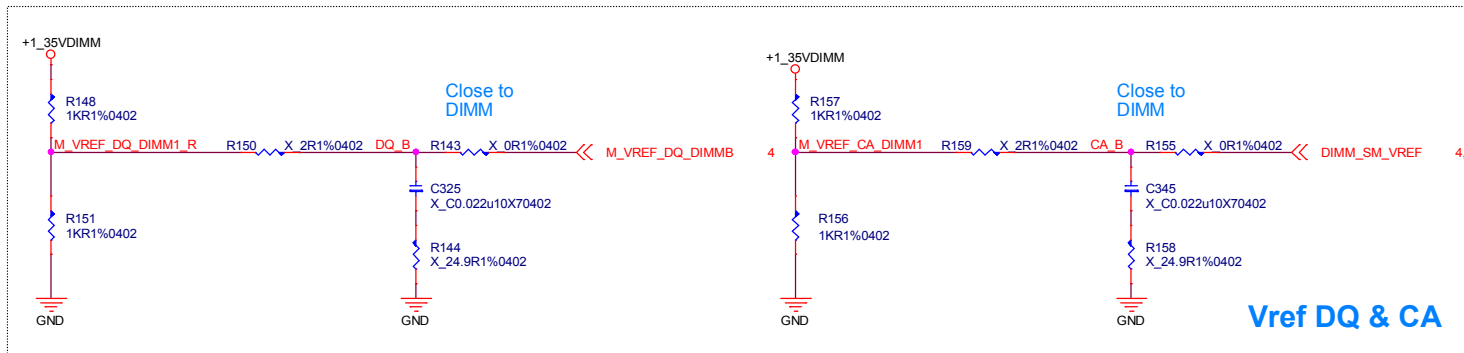
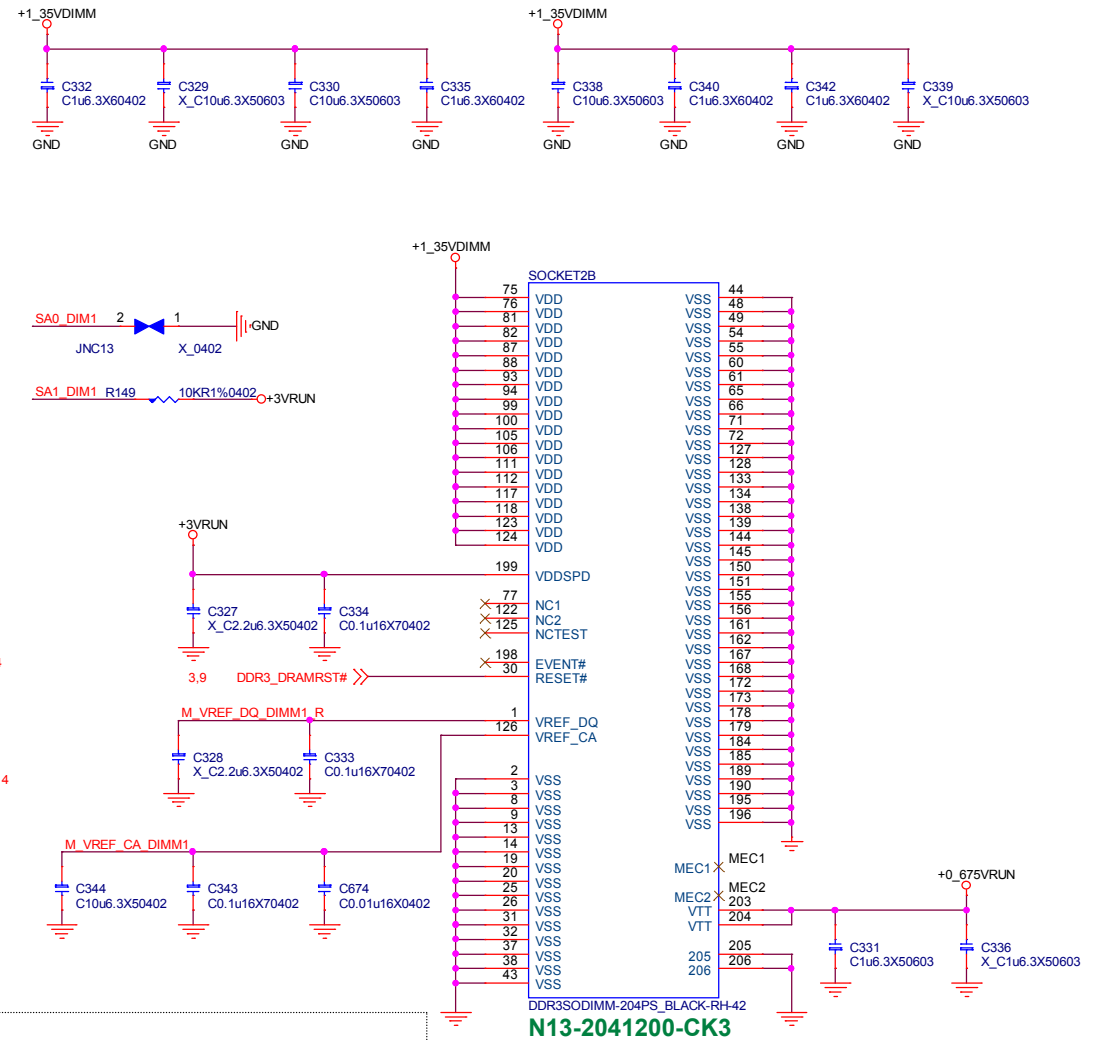
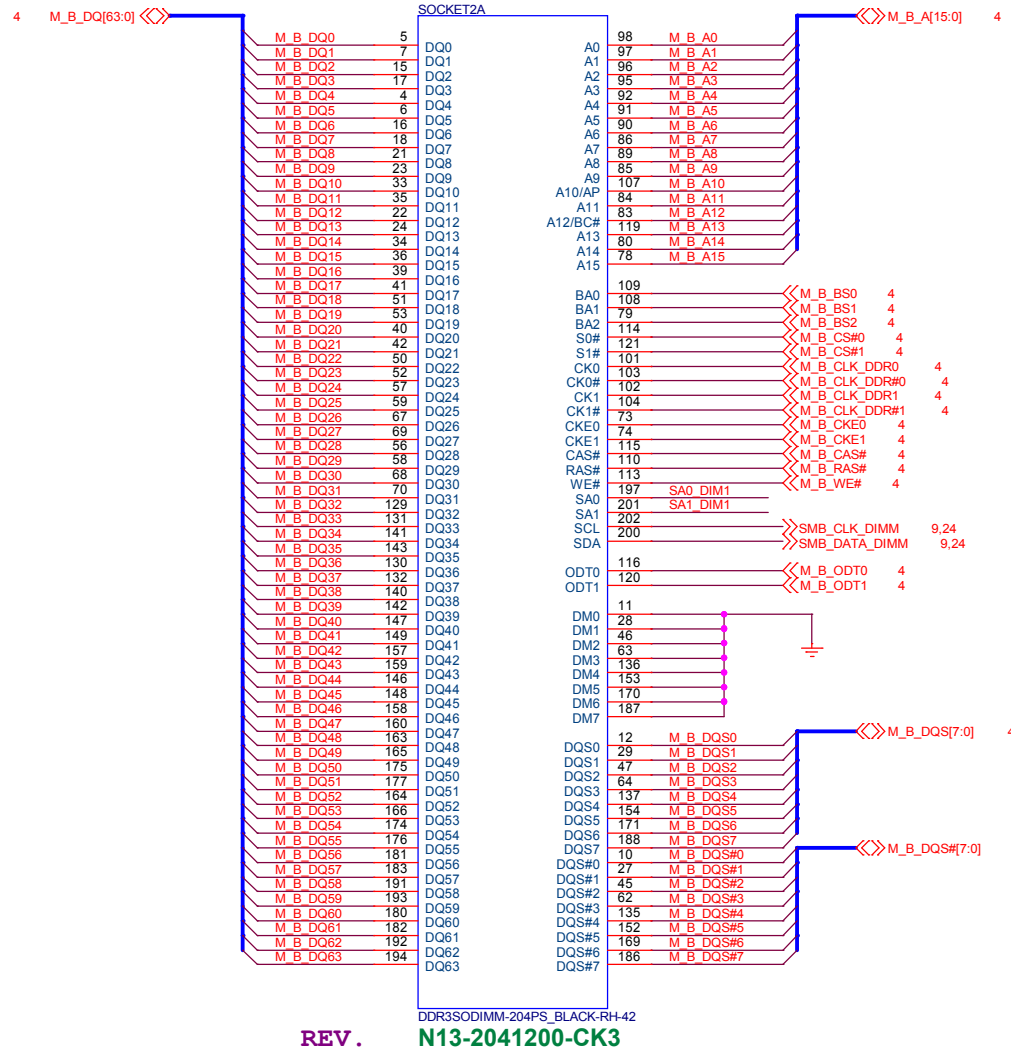
REV. N13-2040750-L41

```
M1 (used for S3)
M3 (used for S0), maybe to over-ride
Active when soft-start
```

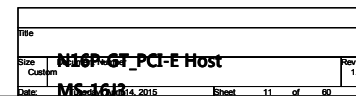


Vref DQ & CA

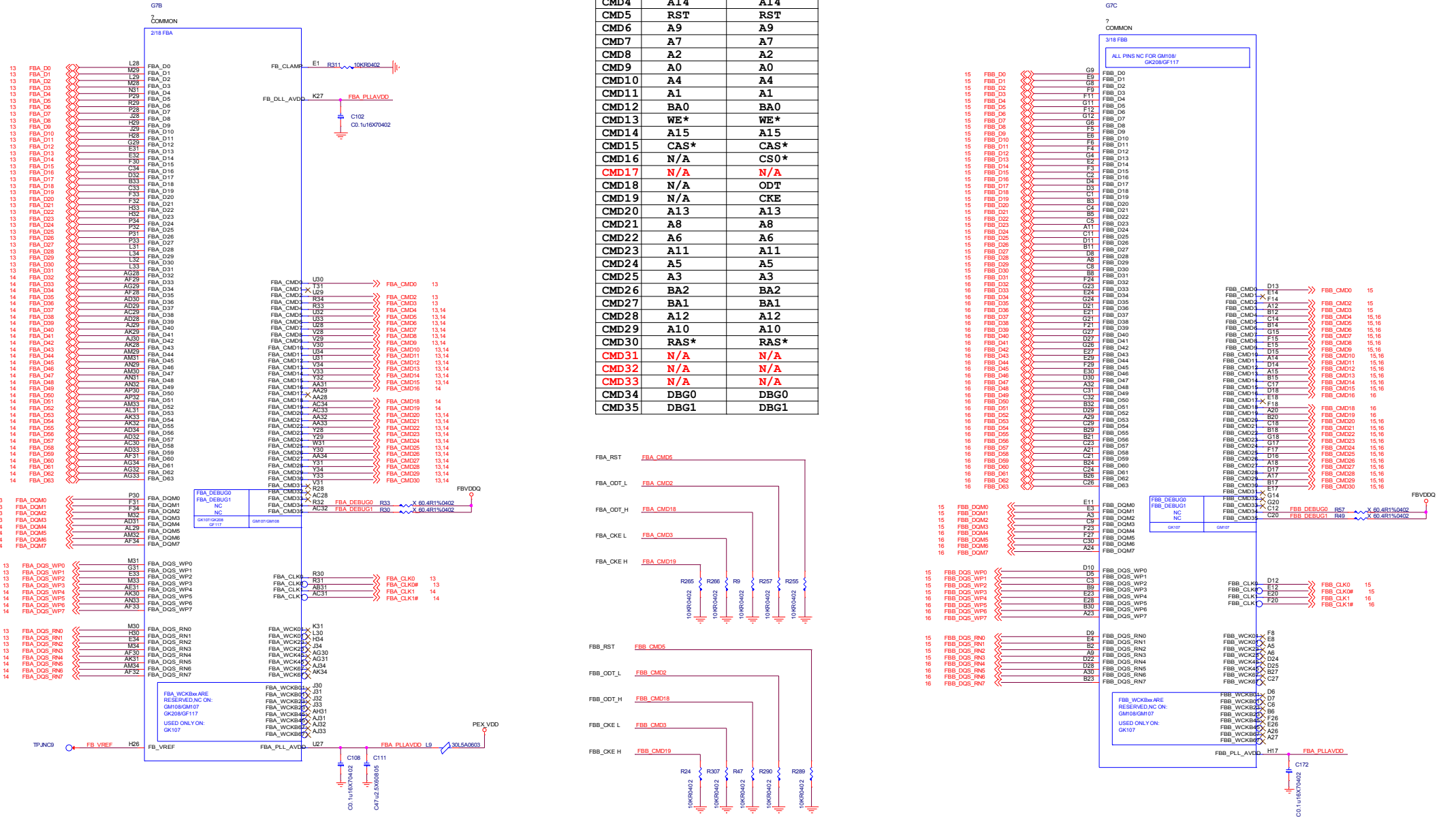
SODIMM#B



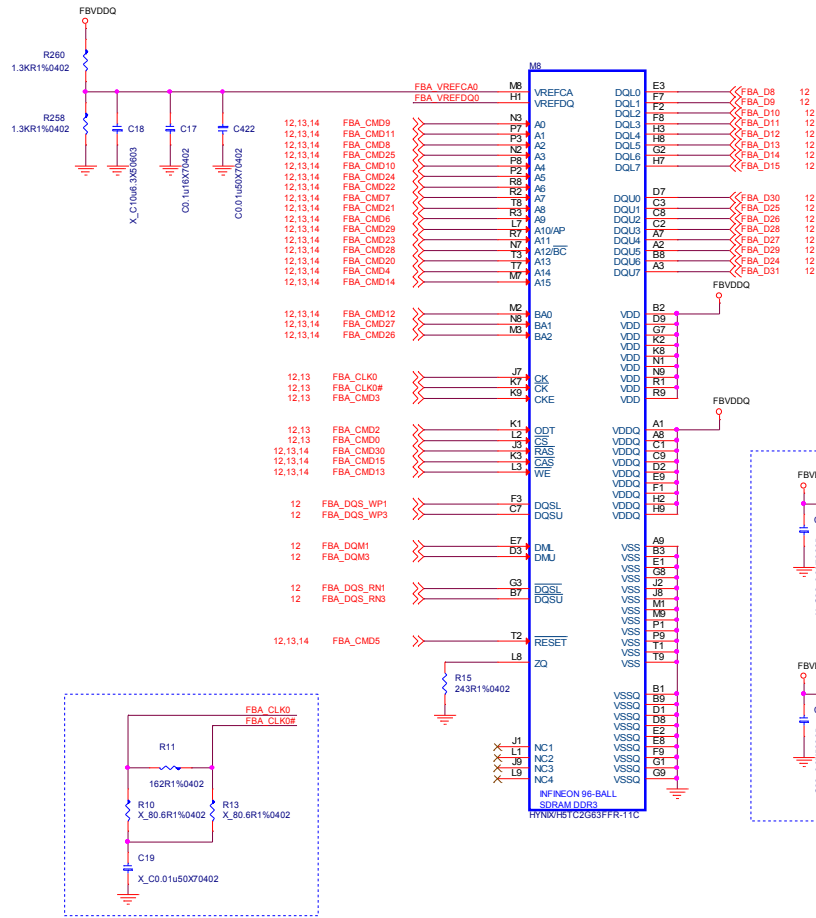
MSI



N16P-GT(Frame Buffer Interface)

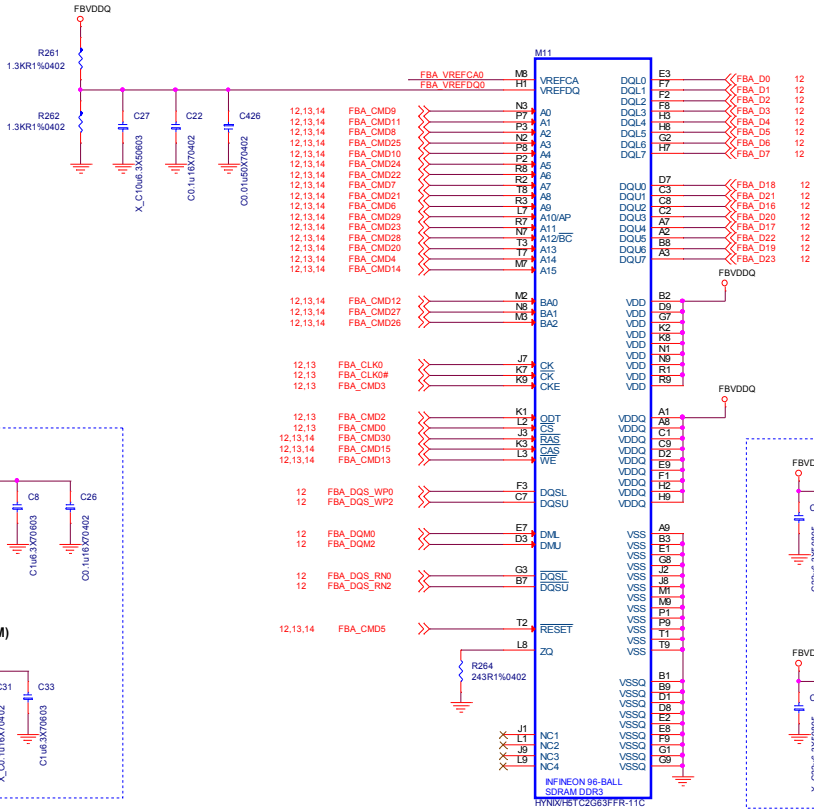
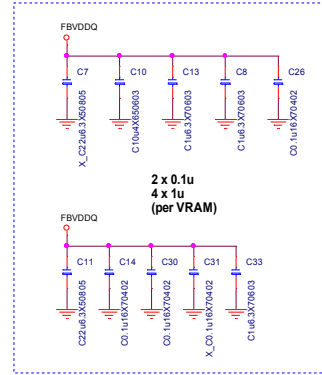


N16P-GT(GDDR3 Frame A-1)



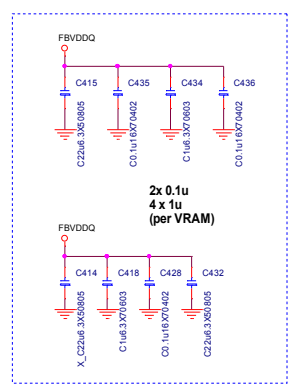
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3



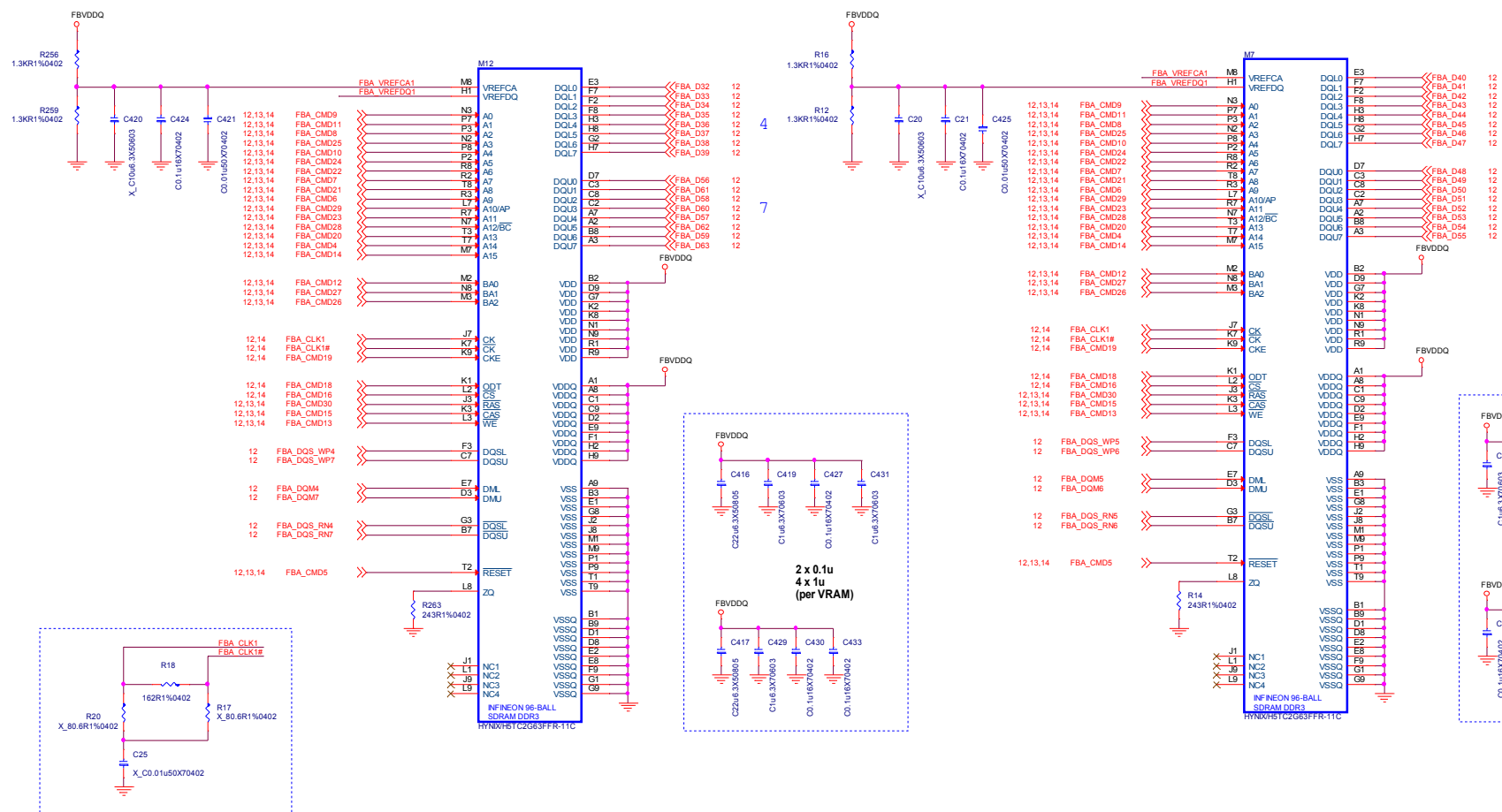
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2

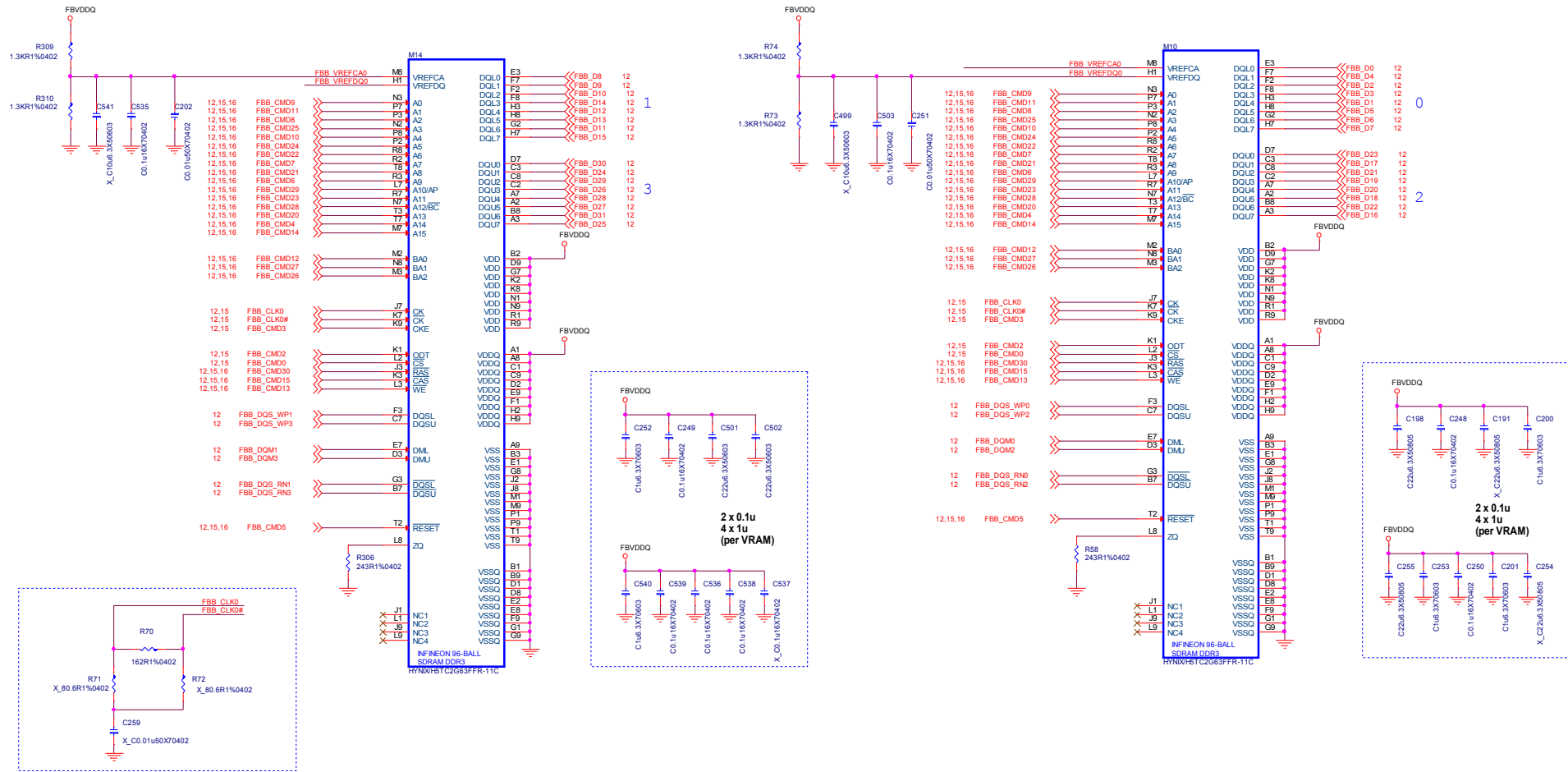


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Size	Document Number		
Customer	MS-1642		
Date	2014.10.14	Sheet	13 of 60

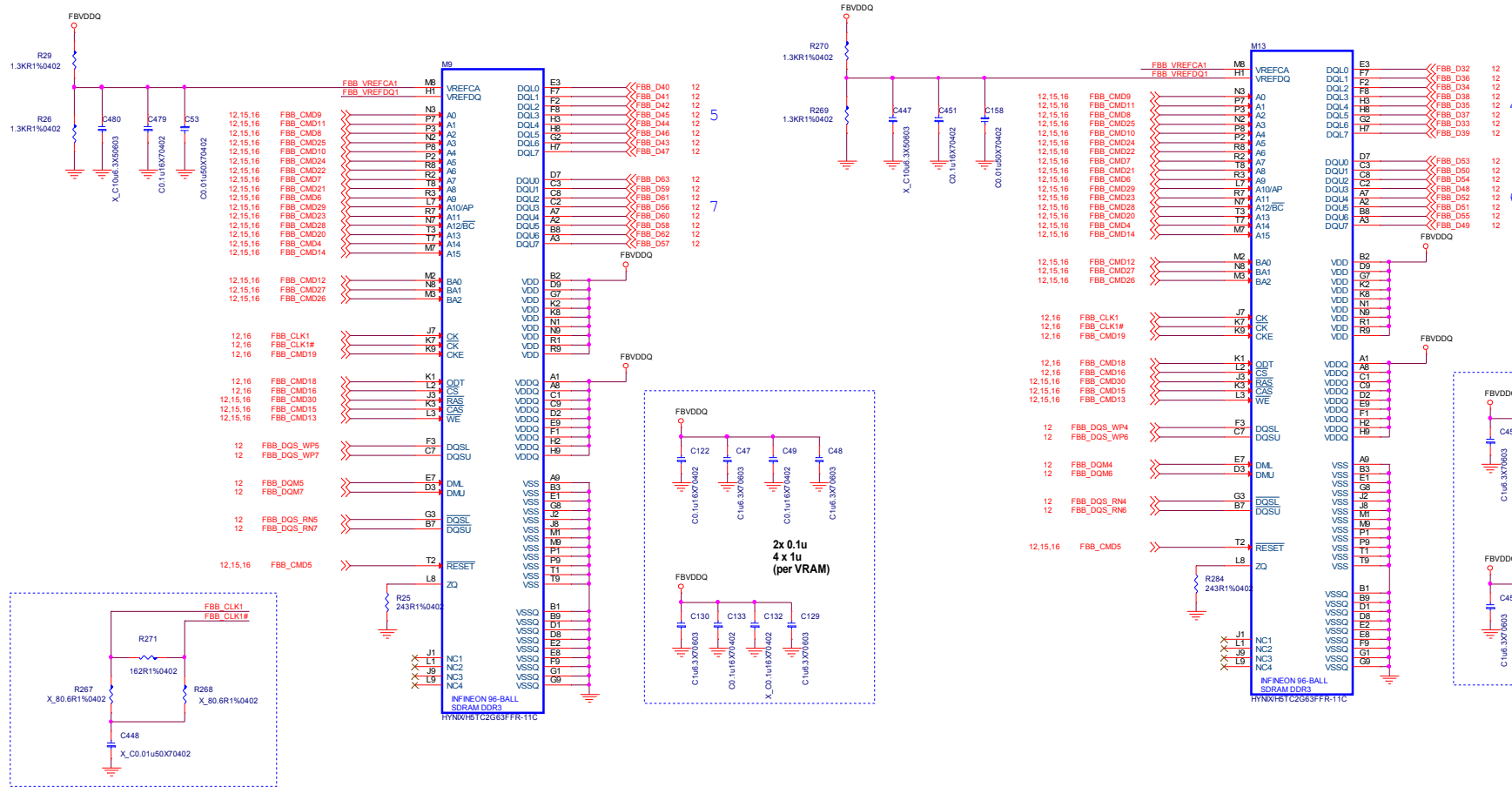
N16P-GT(GDDR3 Frame A-2)



N16P-GT(GDDR3 Frame B-1)



N16P-GT(GDDR3 Frame B-2)

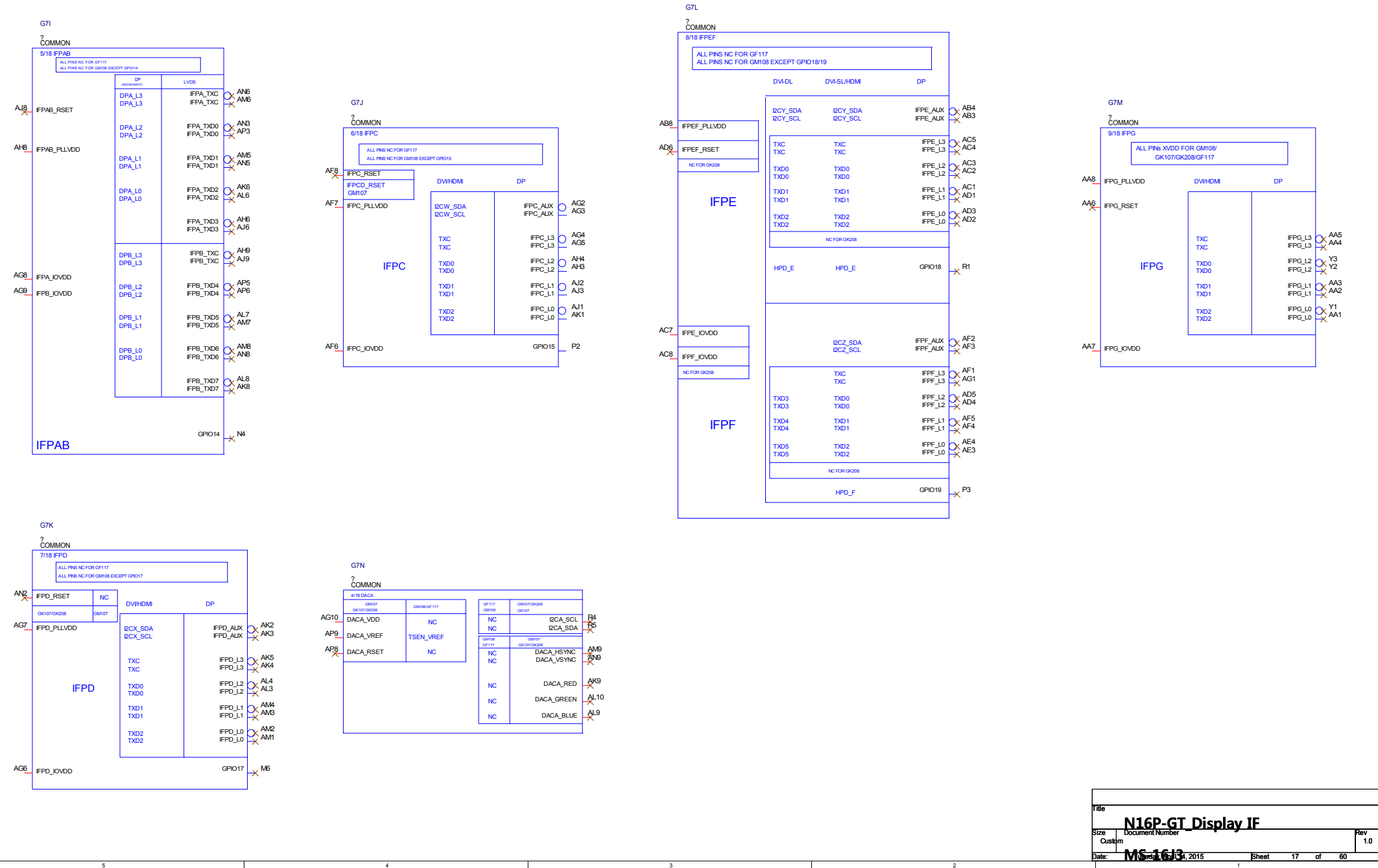


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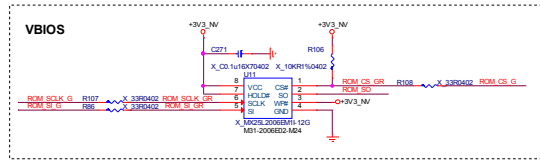
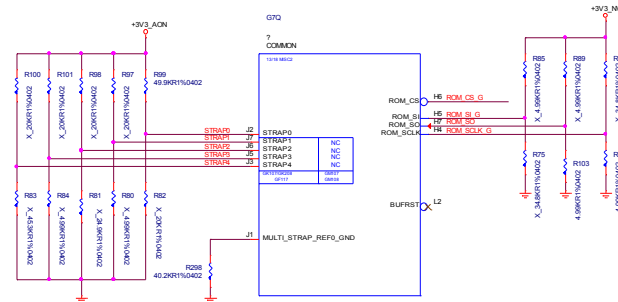
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Date: **March 14, 2015** Sheet: **16** of **60**

N16P-GT(Display IF)



ROM / MULTI-LEVEL STRAPS / GPIO

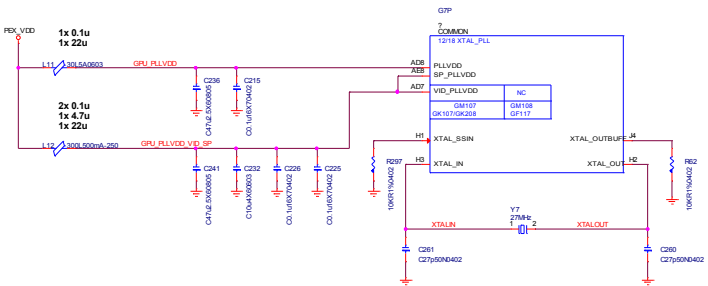


N16P-GT

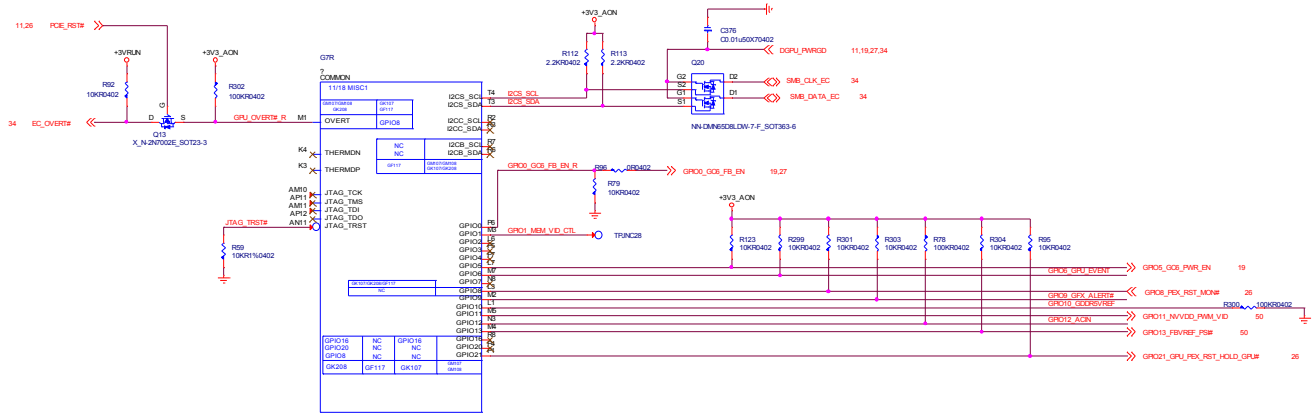
N16S-GT

N16P_GT_2G/N16S_GT_1G			
FC84B8	Hynix	V_T0P1	V_B0T1
R11-3482T12-R01	128Mx16bit	5010	5020
X_34.8KR1%0402		M12-2G63F45-H23	M12-2G63F45-H23
		X_H5TC2G63FFR-11C	X_H5TC2G63FFR-11C
FL84B8	Samsung	V_T0P2	V_B0T2
R11-4991T12-W08	128Mx16bit	5010	5020
X_4.99KR1%0402		M12-K4W2GH5-S02	M12-K4W2GH5-S02
		X_K4W2G1646Q-BC1A	X_K4W2G1646Q-BC1A

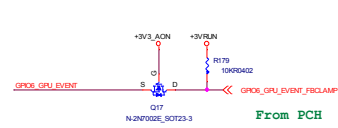
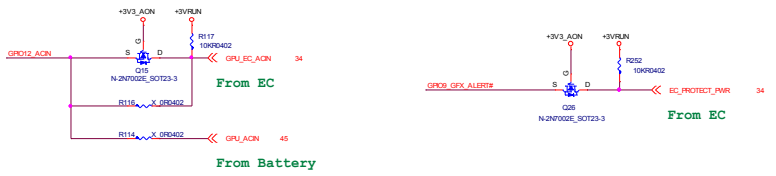
N16P_GT_4G/N16S_GT_2G			
FC84K1	Hynix	V_T0P3	V_B0T3
R11-3012T12-W08	256Mx16bit	5010	5020
X_30.1KR1%0402		M12-4G63C35-H23	M12-4G63C35-H23
		X_H5TC4G63CFR-N0C	X_H5TC4G63CFR-N0C
FC84K	Samsung	V_T0P4	V_B0T4
R11-0153T12-W08	256Mx16bit	5010	5020
X_15KR1%0402		M12-1646D25-S02	M12-1646D25-S02
		X_K4W4G1646D-BC1A	X_K4W4G1646D-BC1A



Item	Location	N16P-GT	N16S-GT	N16S-GM
Device ID		0x139A	0x1347	0x1346
Package		GB4B-128	GB4B-128	GB4B-128
Memory Type		DDR3	DDR3	DDR3
Device Specific Strap Mode Selection	R298	Multi_Strap_Ref0_GND, 40.2K PD to GND	Multi_Strap_Ref0_GND, 40.2K PD to GND	Multi_Strap_Ref0_GND, 40.2K PD to GND
ROM_SI	R85	0x6, Hynix 2G, 34.8kohm pull down	0x6, Hynix 2G, 34.8kohm pull down	0x6, Hynix 2G, 34.8kohm pull down
	R75	0x8, Samsung 2G, 4.99Kohm pull up	0x8, Samsung 2G, 4.99Kohm pull up	0x8, Samsung 2G, 4.99Kohm pull up
		0x9, Hynix 4G, 30.1kohm pull down	0x9, Hynix 4G, 30.1kohm pull down	0x9, Hynix 4G, 30.1kohm pull down
		0x2, Samsung 4G, 15kohm pull down	0x2, Samsung 4G, 15kohm pull down	0x2, Samsung 4G, 15kohm pull down
ROM_SO	R103	4.99Kohm pull down	4.99Kohm pull down	4.99Kohm pull down
ROM_SCLK	R102	4.99Kohm pull down	4.99Kohm pull down	4.99Kohm pull down
Strap0	R99	49.9Kohm pull up	49.9Kohm pull up	49.9Kohm pull up
Strap1		NC	NC	NC
Strap2		NC	NC	NC
Strap3		NC	NC	NC
Strap4		NC	NC	NC

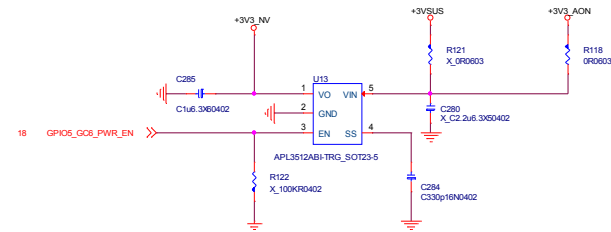


Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPI00	GC6_FB_EN(GPI00_GC6_FB_EN)	O	FB Enable for GC6 2.0	10K pull-down
GPI01	MEM_VDD_CTL(NC)	O	Memory VDD VID	
GPI02	LCD_BL_PWM(NC)	O	Panel Backlight PWM Brightness Control	
GPI03	LCD_VCC(NC)	O	Panel Power Enable	
GPI04	LCD_BLEN(NC)	O	Panel Backlight Enable	
GPI05	3V3_MAIN_EN(GPI05_GC6_PWR_EN)	O	GPU POWER Sequencing	10K pull-up to 3V3_AON
GPI06	GPU_EVENT#(GPI06_GPU_EVENT_FBClamp)	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3_AON
GPI07	3DVision(NC)	O	3D Vision L/R signal	
GPI08	SYS_PEX_RST_MON#(GPI08_PEX_RST_MON#)	I	System side PCI reset Monitor	10K pull-up to 3V3_AON
GPI09	ALERT(EC_PROTECT_PWR)	I/O	Active Low Thermal Alert	10K pull-up to 3V3_AON
GPI010	MEM_VREF_CTL(GPI010_GDDR5VREF)	O	Memory VREF Control	100K pull-down
GPI011	PWR_VID(GPI011_GPUVID)	O	GPU Core VDD PWM control signal	
GPI012	PWR_LEVEL(GPI012_ACIN)	I	AC power detect or power supply Overdraw Input	100K pull-up to 3V3_AON
GPI013	PSI(GPI013_FBVREF_FSI#)	O	Phase shedding	10K pull-up to 3V3_AON
GPI014	HPD_A(NC)	I	Hot Plug Detect for IPFA used as DisplayPort or for IPFAB when used as Dual Link DVI	
GPI015	HPD_C(NC)	I	Hot Plug Detect for IPFC	
GPI016	FRAME_LOCK#(NC)	I	Active Low Frame Lock	
GPI017	HPD_D(NC)	I	Hot Plug Detect for IPFP	
GPI018	HPD_E(NC)	I	Hot Plug Detect for IPFP	
GPI019	HPD_F or HPD_B(NC)	I	Hot Plug Detect for IPFP or for IPFB when used as DisplayPort	
GPI020	RESERVED			
GPI021	GPU_PEX_RST_HOLD (GPI021_GPU_PEX_RST_HOLD_GPU#)	O	GPU PCIe self-reset control	10K pull-up to 3V3_AON
OVERT	OVERT(OVERT#)	O	Active Low Catastrophic Over Temperature	100K pull-up to 3V3_AON

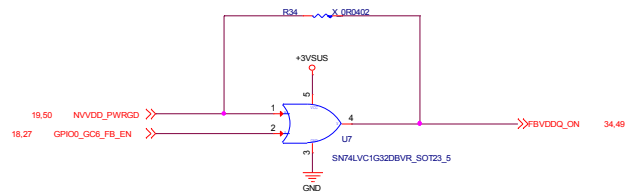


+3V3_AON -> +3V3_NV -> NVVDD -> PEX_VDD -> FBVDDQ -> DGPUPWRGD

The schematic diagram illustrates the power management section of the iSB-LDW-7-F-S0T363-6. It shows the connection of various power sources (PWR_SRC, +3V_SUS, +3V_AON, +3V_VN) to the board's internal components. Key components include resistors (RPS4, RPS1, RPS2, R110, R468, R469, R470), capacitors (X100K0R0402, X47KR1%0402, X47KR1%0402, X150D070402, X2MR0402, X2MR0402, XN27002_S0T23-3), and a diode (D1). The diagram also shows the connection of the PLT_RST# signal to the board's internal components. Annotations include 'add PLT_RST# to avoid 3V3_NV Leakage' and 'Disable GC6'.



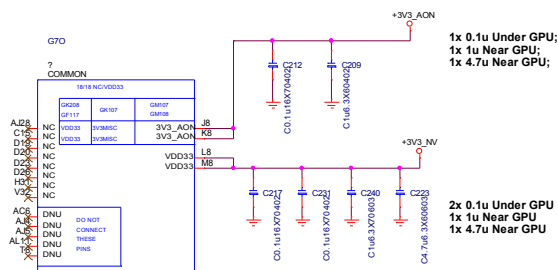
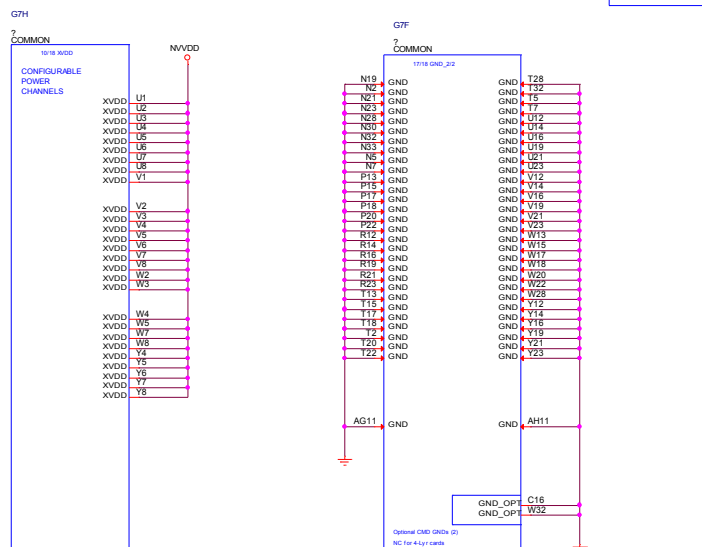
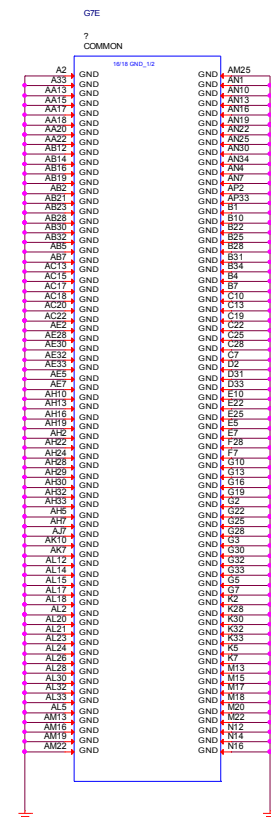
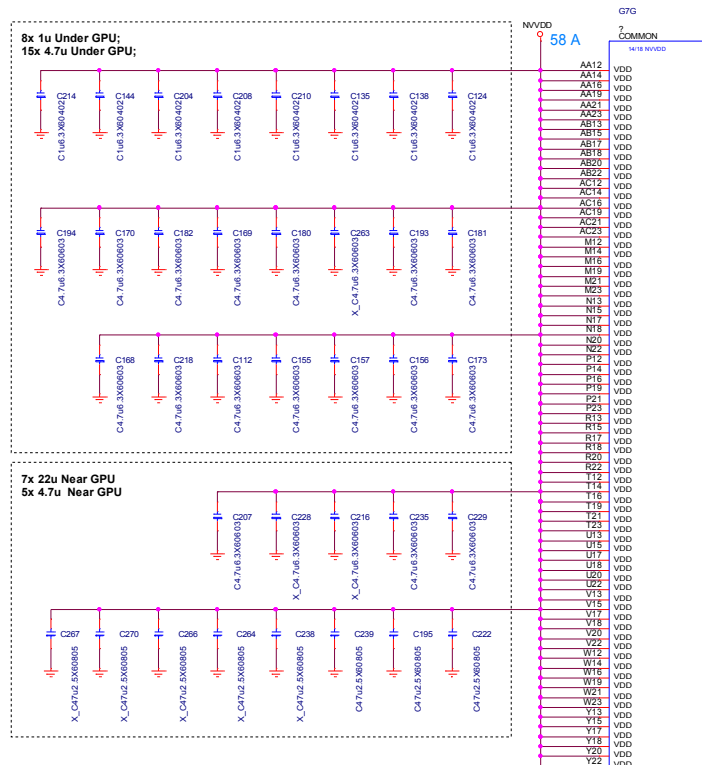
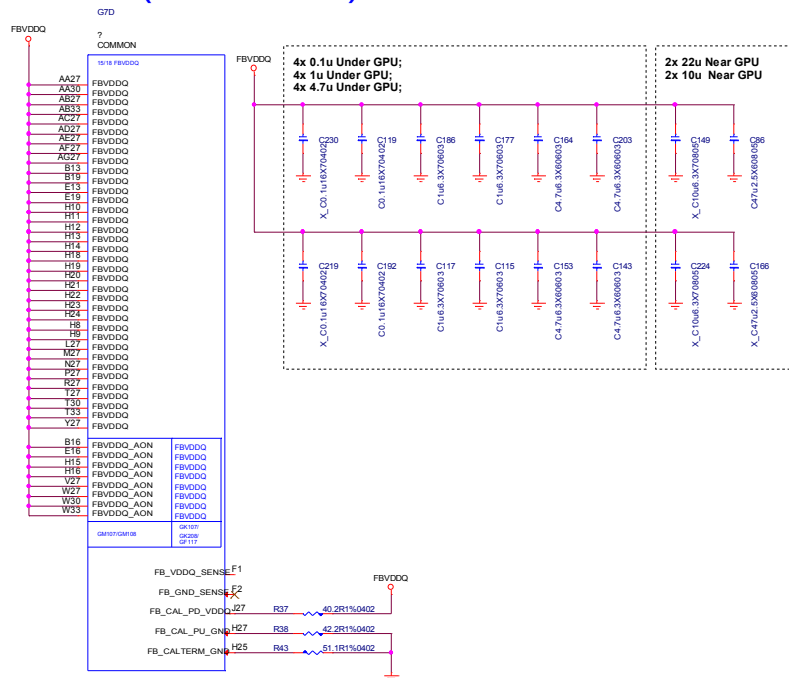
Disable GC6

[illegible]

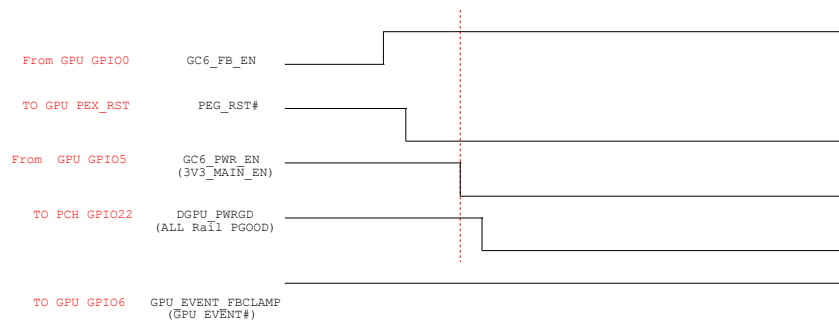
The schematic shows the power supply circuitry for the PEX6800 evaluation board. It includes several input sources: +V3_1V, +5VSUS, PWR_SRC, +1.05VRUN, and DGPU_PWR_EN#. The +V3_1V source passes through PR26 (23.4K R1%0402) to PC17 (C0.1uF X7R0402), which is connected to GND. The +5VSUS source passes through PR28 (100K F0402) to the gate of MOSFET PQ12 (NN-OMN650RLDW-7-F_SOT23-6). The PWR_SRC source passes through PR27 (62KR1%0402) to the drain of PQ12. A feedback network consisting of PR29 (470KR1%0402) and PC18 (C2200p50X70402) connects the output node to the gate of PQ12. The output of PQ12 is labeled "+1.05VRUN ON". This signal is also connected to the gate of MOSFET Q7 (N-AON7516_DFN3X3). The DGPU_PWR_EN# signal is connected to the gate of MOSFET PQ11 (N-N7002_SOT23-3). The output of Q7 is labeled "PEX_VDD" and has a current rating of 3.5A. A decoupling capacitor CQ4 (C0.1uF X7R0402) is connected between the output and ground.

The schematic diagram illustrates the NVDD_PWRGD signal path. It starts with the FIBVDDQ signal, which passes through a resistor network (R76, R77, R78) and a buffer (Q12) to the input of a Schmitt trigger (U10). The output of U10 is connected to the NVDD_PWRGD signal. The circuit is powered by +3VSUS and includes decoupling capacitors C262 and C256.

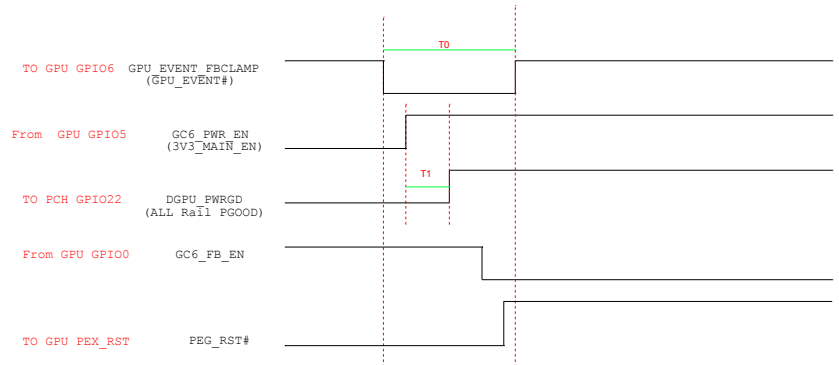
N16P-GT(Power & GND)



GC6 2.0 ENTRY SEQUENCE



GC6 2.0 EXIT SEQUENCE



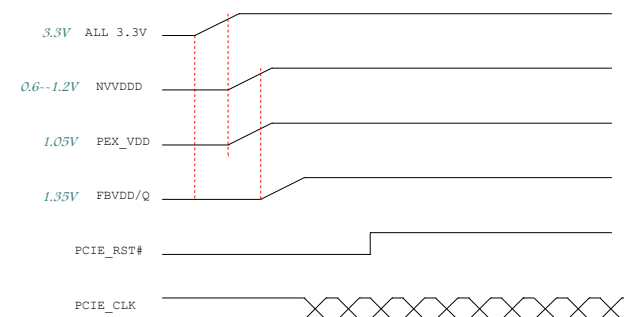
GC6 2.0 TIMING

	Min	Max	Unit	Description
T0	0.001	N/A	mS	GPU_EVENT# assertion
T1	0.04	4	mS	3V3_MAIN_EN assertion to all power rails up and stable

NOTES:

1. ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation.
If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
2. During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
3. All delays should be minimized to increase time spent in GC6 for maximum power saving.
4. The entire entry and exit sequence must complete within 200 ms.

GPU POWER ON SEQUENCE

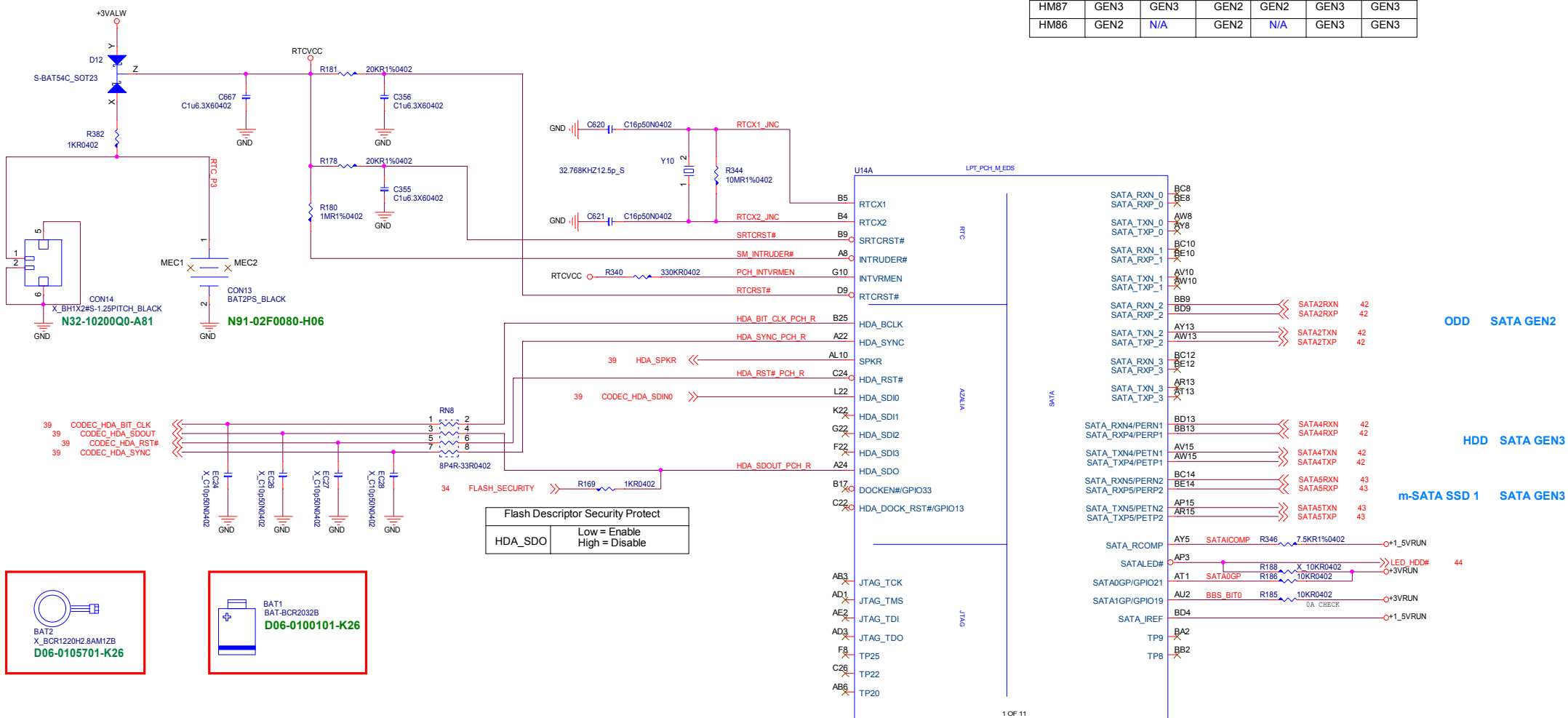


NOTES:

1. The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
2. The ramp up overshoot should not exceed the silicon reliability limit voltage.
3. A VDD33 must ramp up to 90% before NVVDD and PEX_VDD in sequence can ramping up.
NVVDD must ramp up to 90% before FBVDD/Q in sequence can ramping up.
3. No signal should be applied to the GPU before the power rails are fully ramped.
4. Refer to JEDEC Memory Specification for memory related power sequencing.

Lynx Point (HDA/JTAG/SATA)

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3

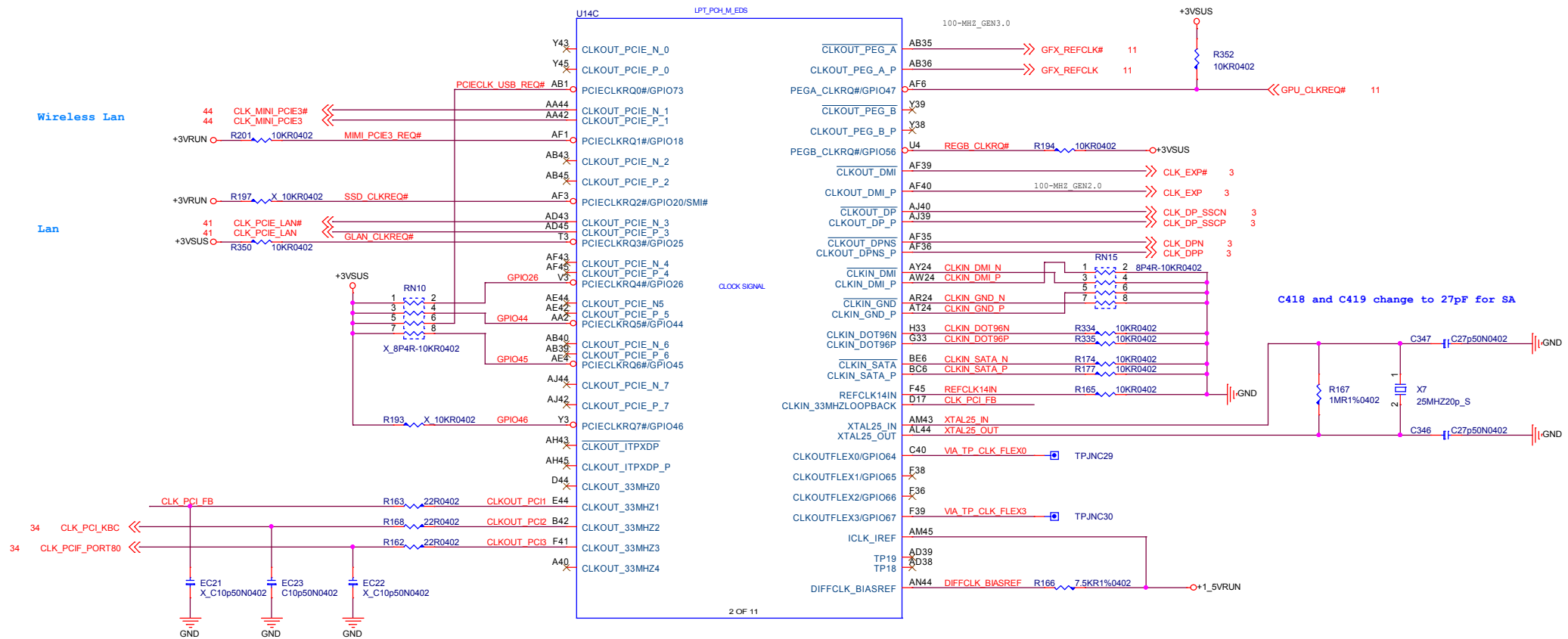


SPK	<p>The Signal has a weak internal pull-down</p> <p>Note: the internal pull-down is disabled after PLTRST# deasserts.</p> <p>If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)</p>
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Lynx Point (Clock)

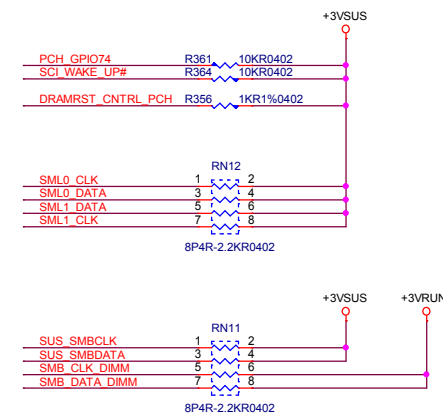
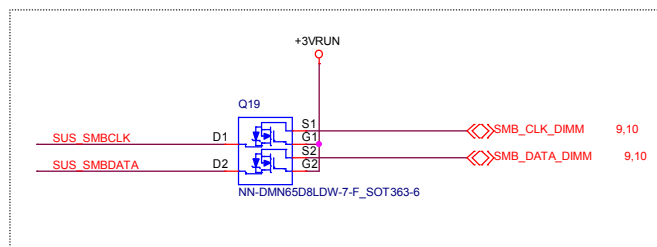
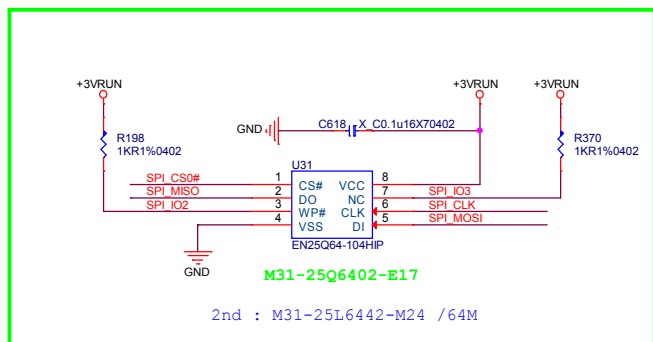
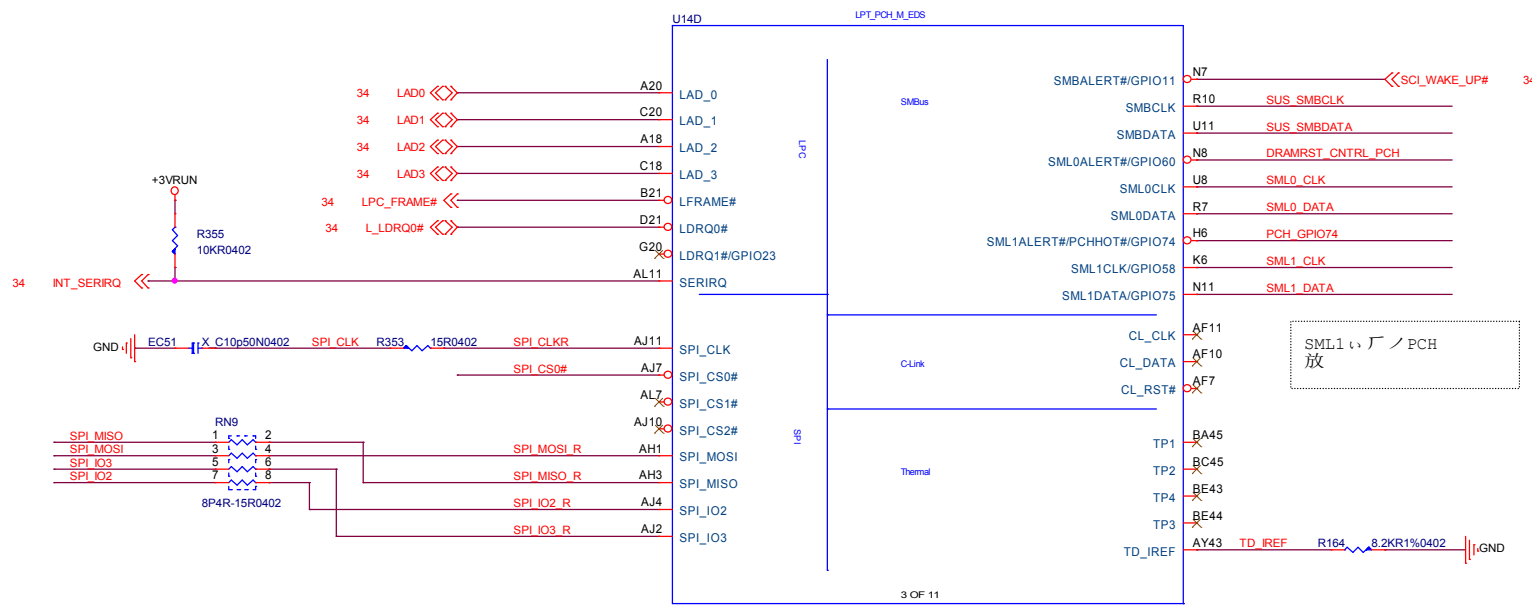
PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 k Ω 10% external pull-up resistor instead of No Connect.

Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

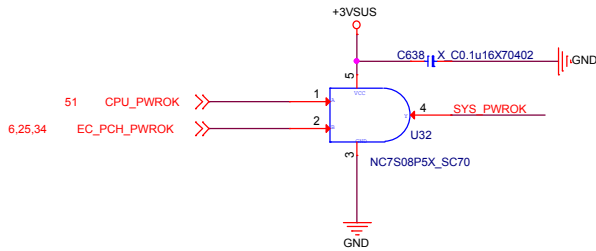
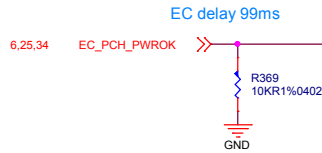
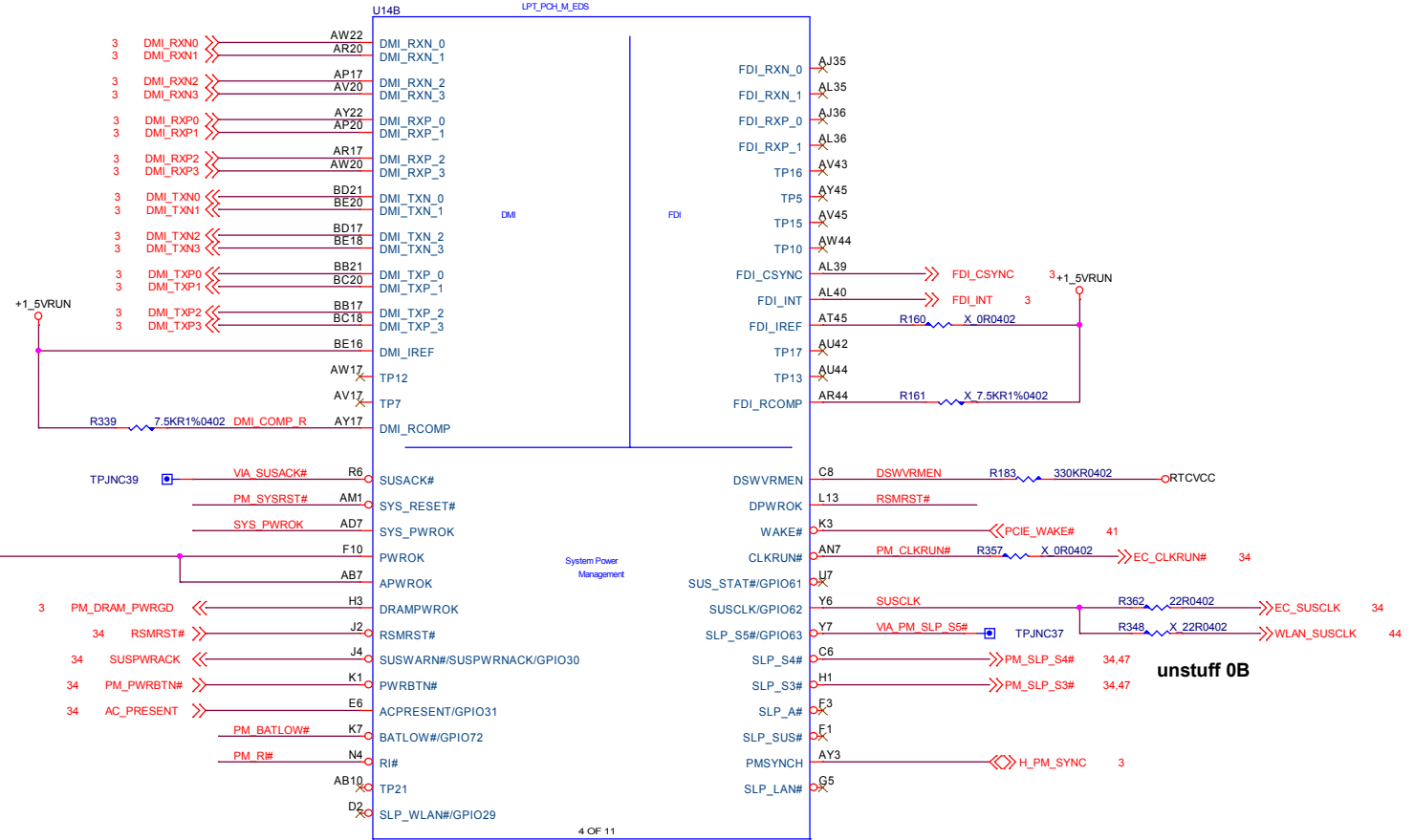
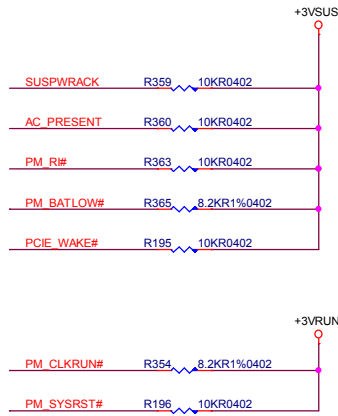


The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

Lynx Point (LPC,SMBUS)



Lynx Point (DMI,FDI)

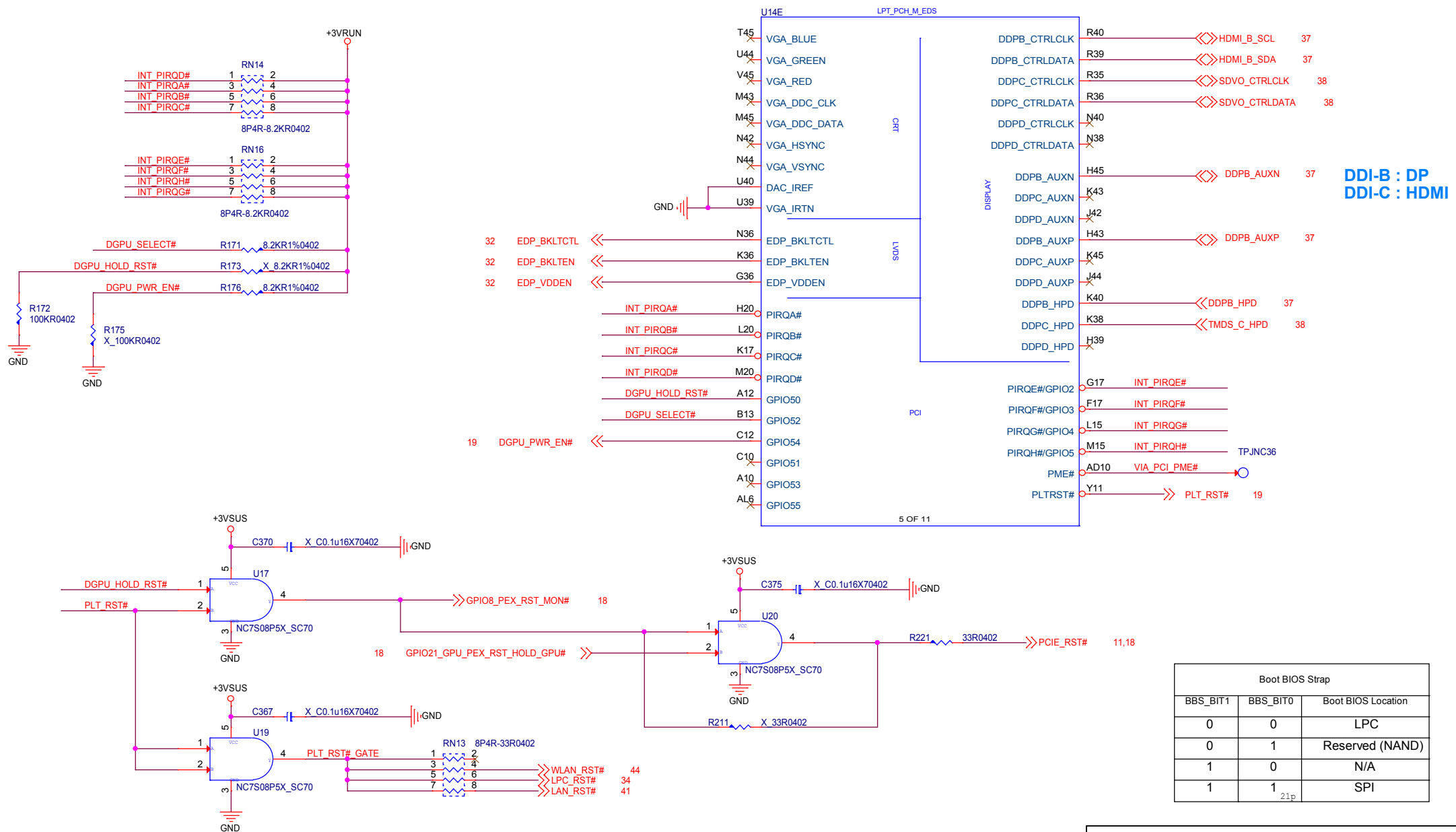


APWROK not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSWMRST - On Die DSW VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

GPIO Setting : Ref 486708_LPT_EDS Section2.18

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

Lynx Point (PCI,DDI)

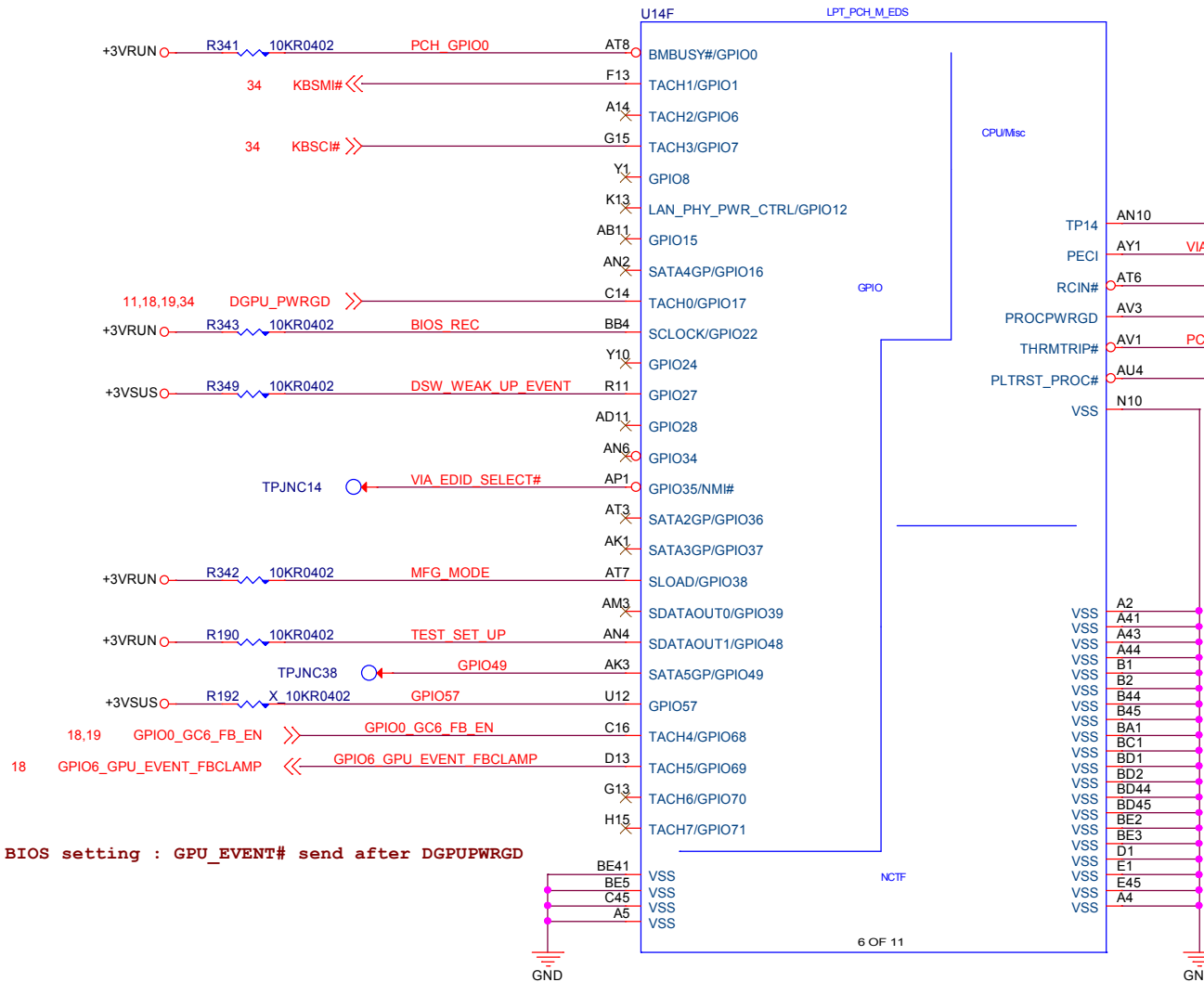


Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1 _{21p}	SPI

Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

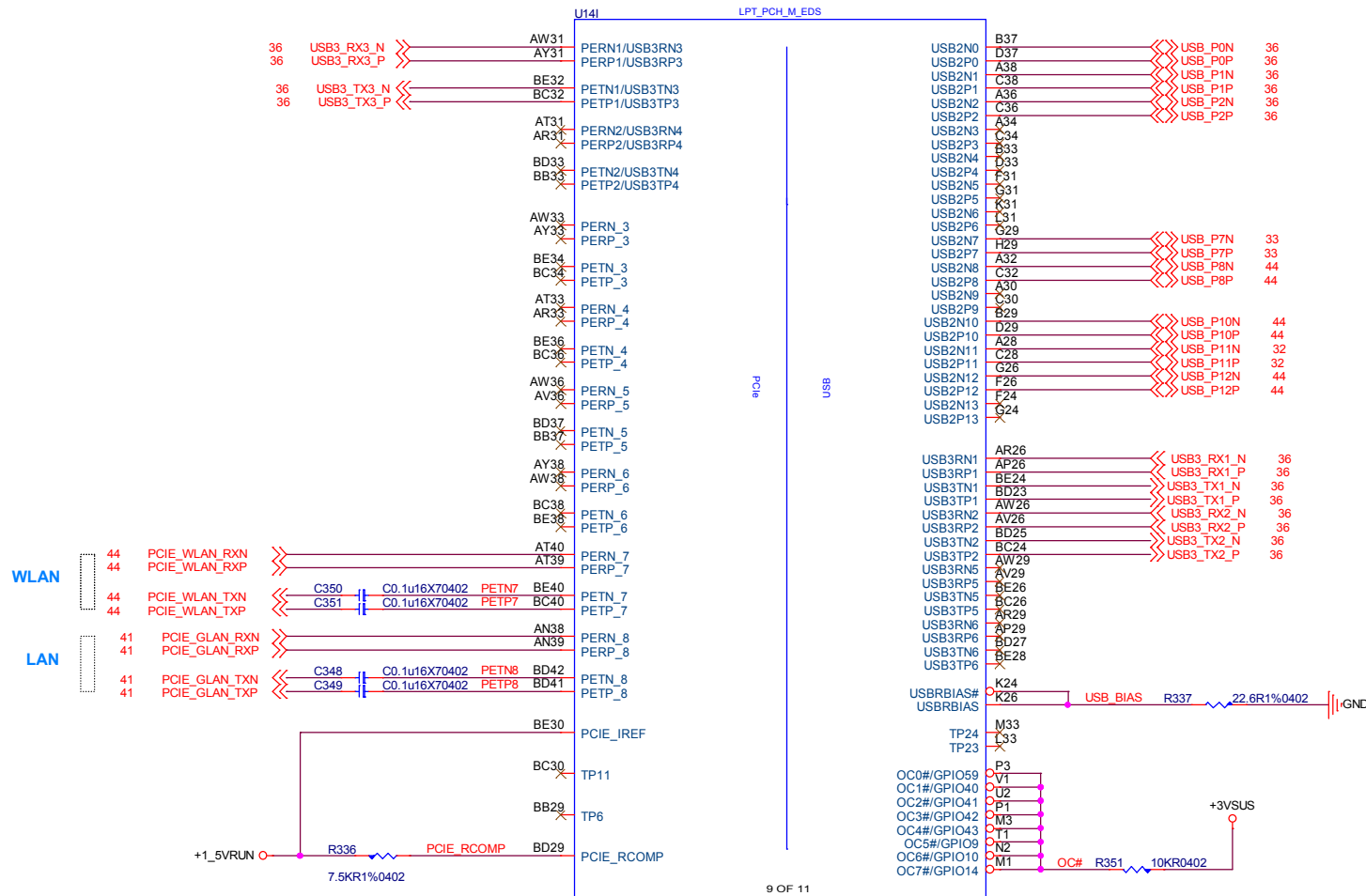


THRMTRIP# Setting : 486713_Shark_Bay_Mobile_PDG

THRMTRIP#	
Haswell	NC
Broadwell	Pull High

Lynx Point (PCIE,USB)

Intel Lynx Point ECHI USB(2.0) debug transport 惠铂Port1 or Port9



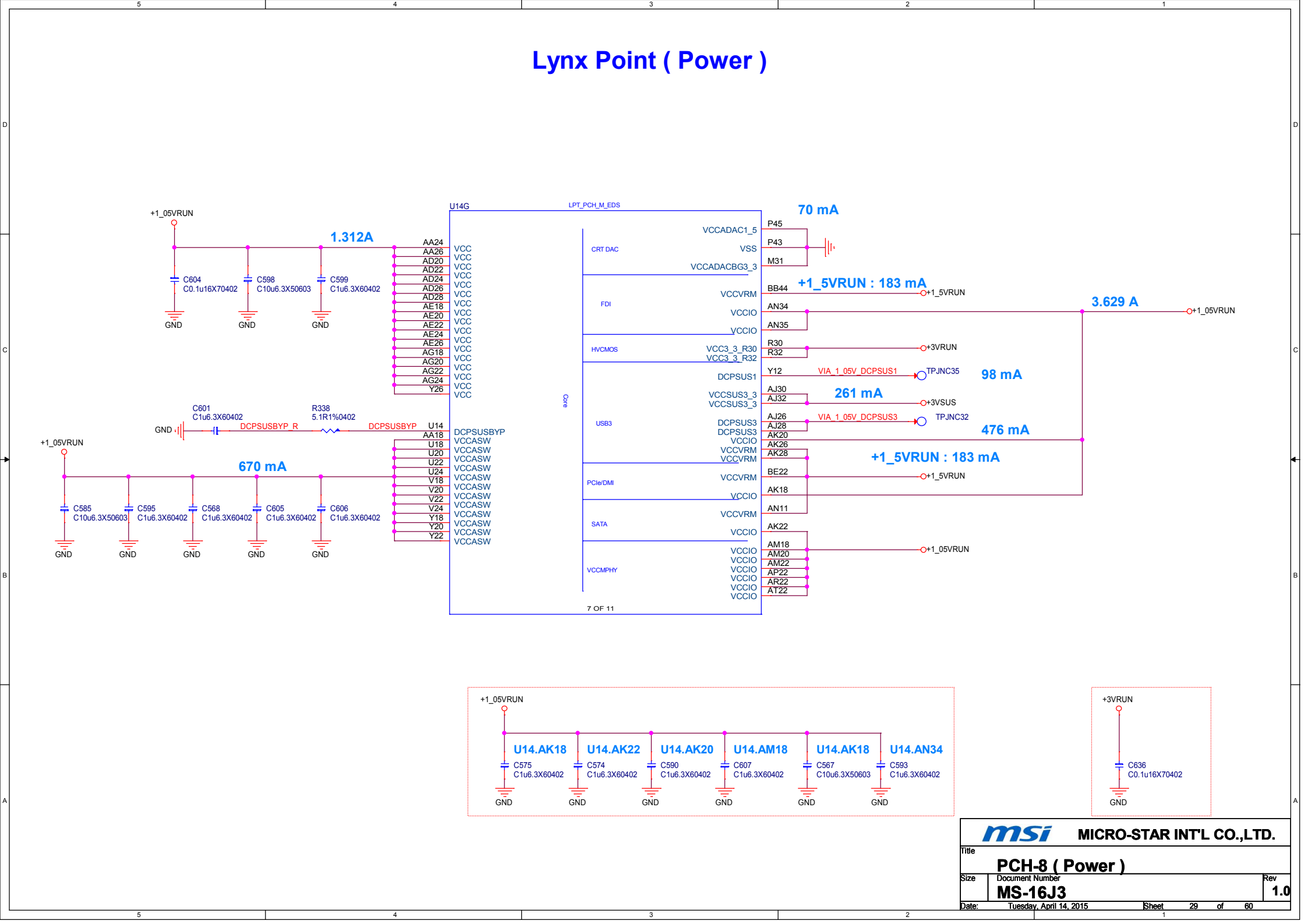
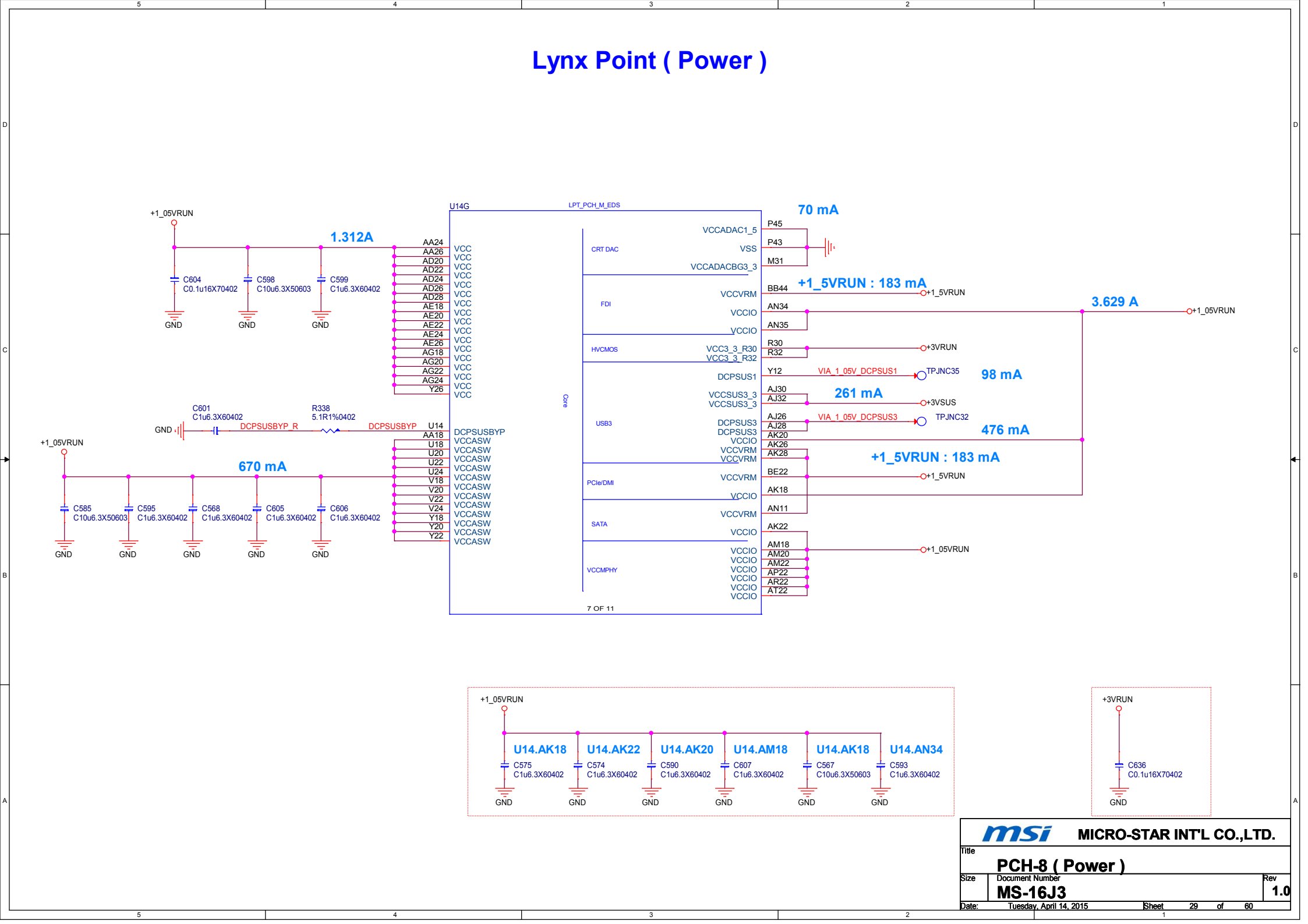
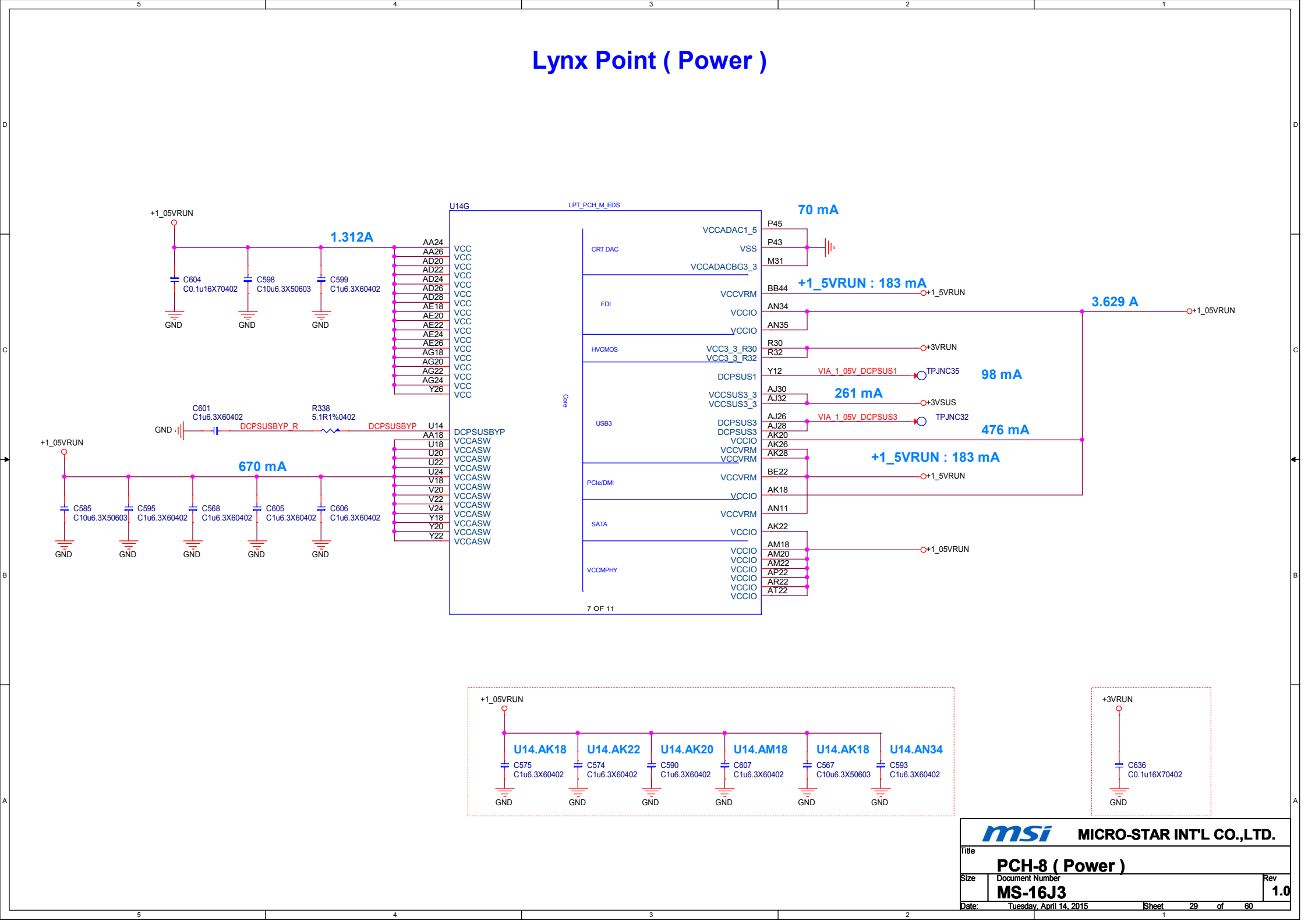
USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	16J31
1	2	USB 3.0 Port 2	16J31
2	3	USB 3.0 Port 3	16J31
3			
4			
5			
6			
7		EPF021	
8		USB 2.0	16J12
9			
10		WLAN	
11		WebCam	
12		CARDREADER	16J12
13			

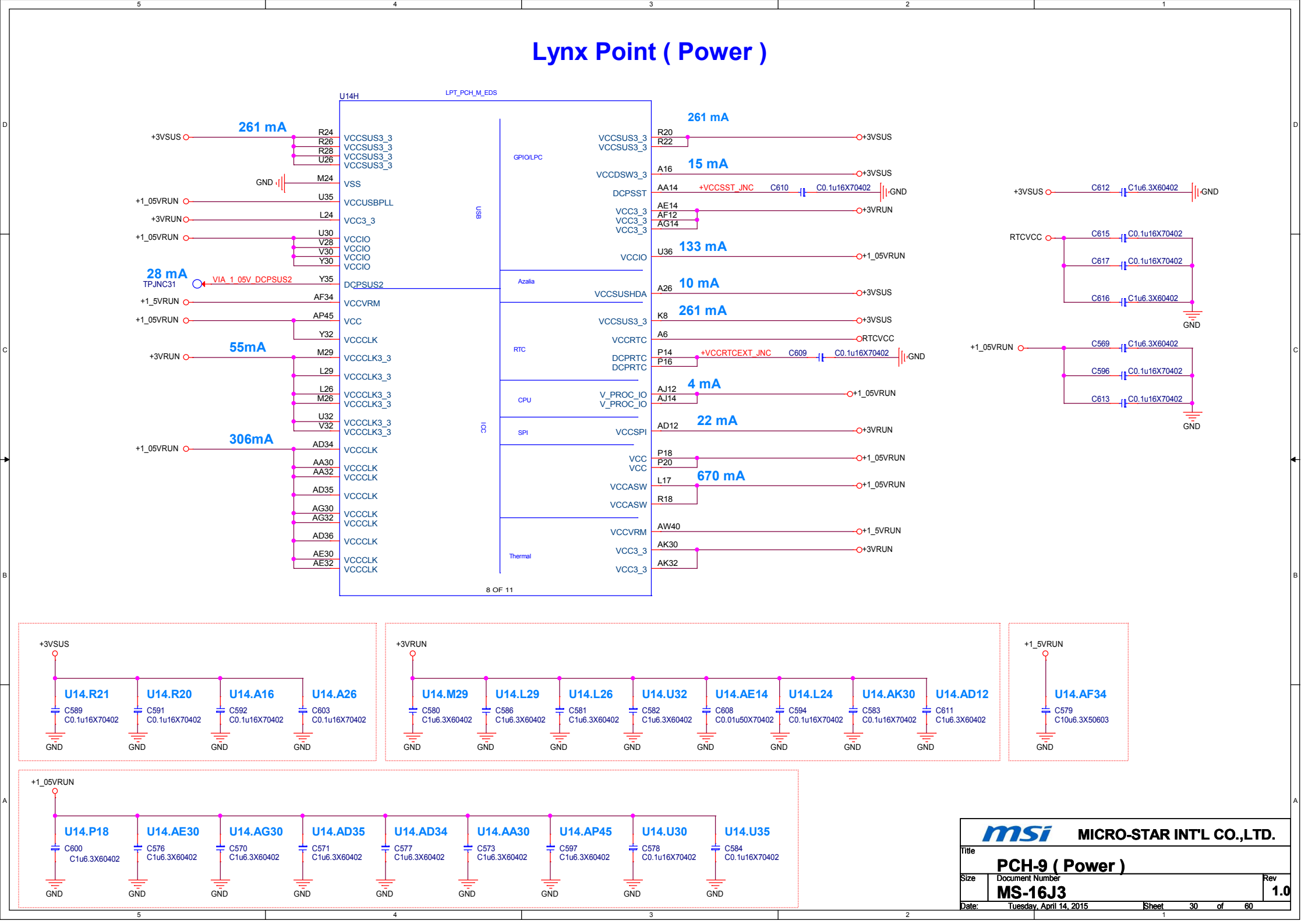
USB 2.0	USB 3.0
0	1
1	2
2	3
3	4
8	5
9	6

SKU	High Speed USB 3.0 I/O Ports					
	USB 3.0-1	USB 3.0-2	USB 3.0-3	USB 3.0-4	USB 3.0-5	USB 3.0-6
HM87	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0
			PCI-E	PCI-E		
HM86	USB 3.0	USB 3.0	USB 3.0	USB 3.0	N/A	N/A
			PCI-E	PCI-E		

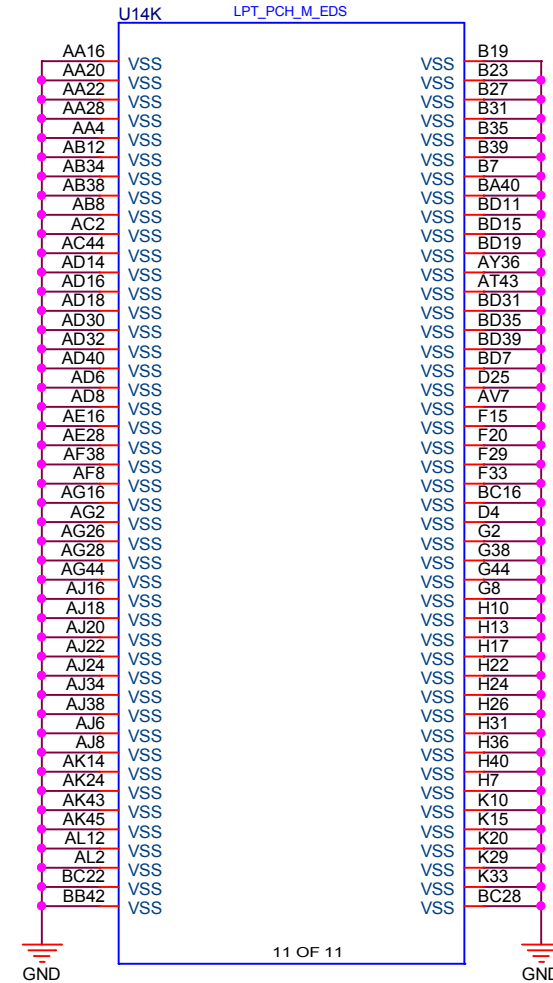
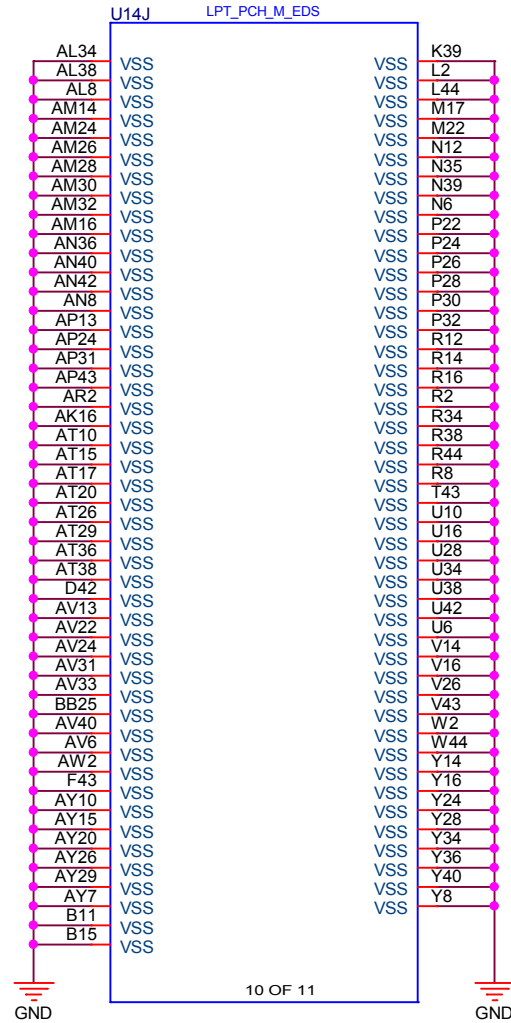
msi MICRO-STAR INT'L CO.,LTD.

Title			
PCH-7 (PCIE,USB)			
Size	Document Number	Rev	
	MS-16J3	1.0	
Date:	Tuesday, April 14, 2015	Sheet	28 of 60

[illegible]

[illegible]

Lynx Point (GND)

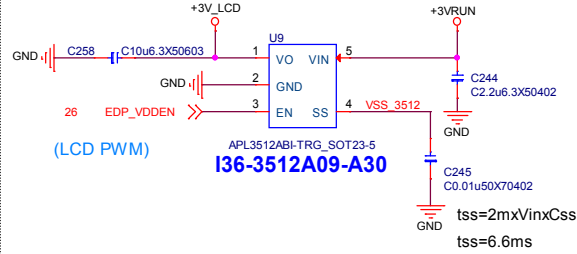


MICRO-STAR INT'L CO.,LTD.

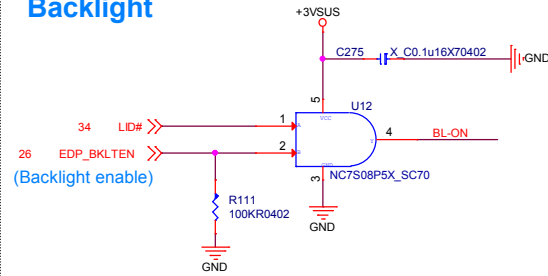
Title		
PCH-10 (GND)		
Size	Document Number	Rev
	MS-16J3	1.0
Date:	Tuesday, April 14, 2015	Sheet 31 of 60

eDP

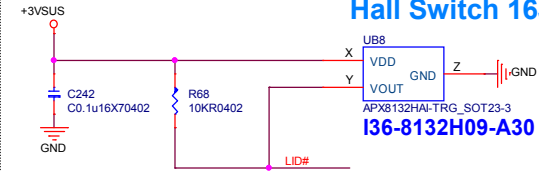
Pannel Device Logic Power



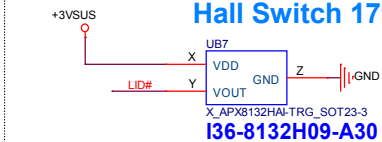
Backlight



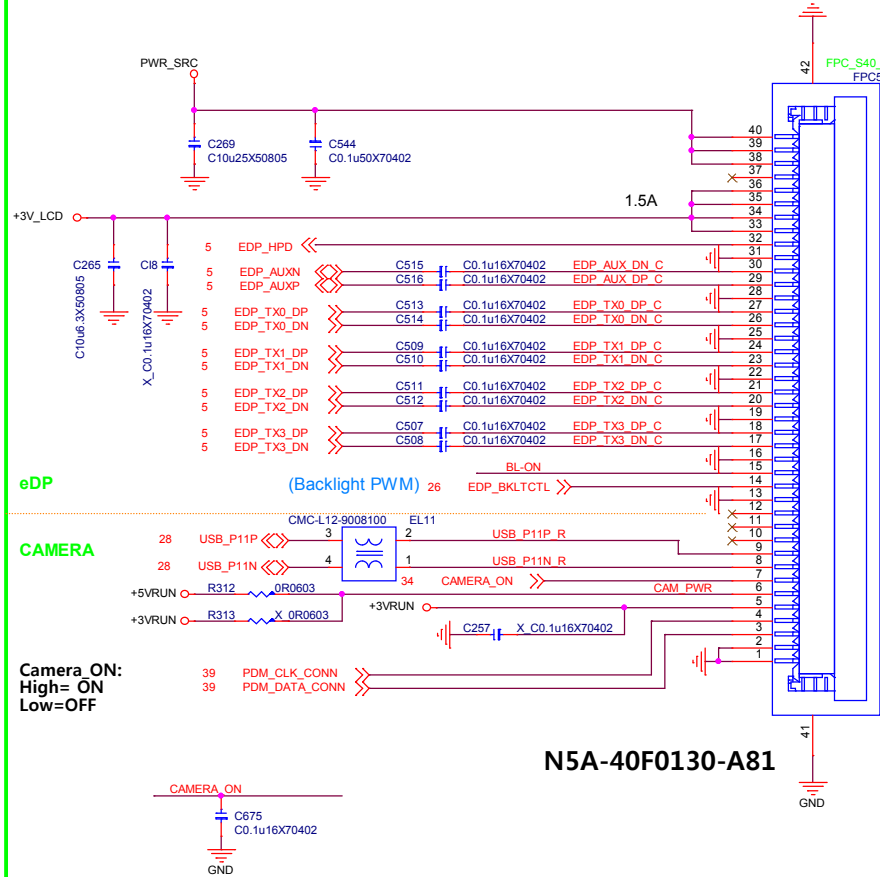
Hall Switch 16J3



Hall Switch 1793

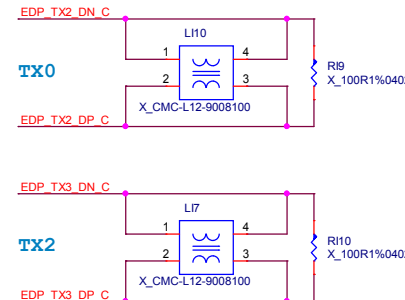
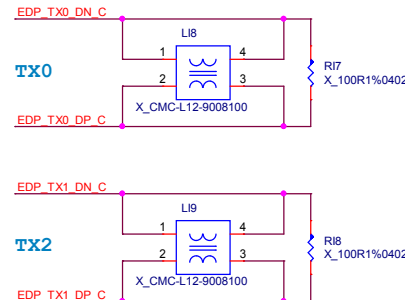


eDP CONN CAMERA



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPDC	HPDC signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

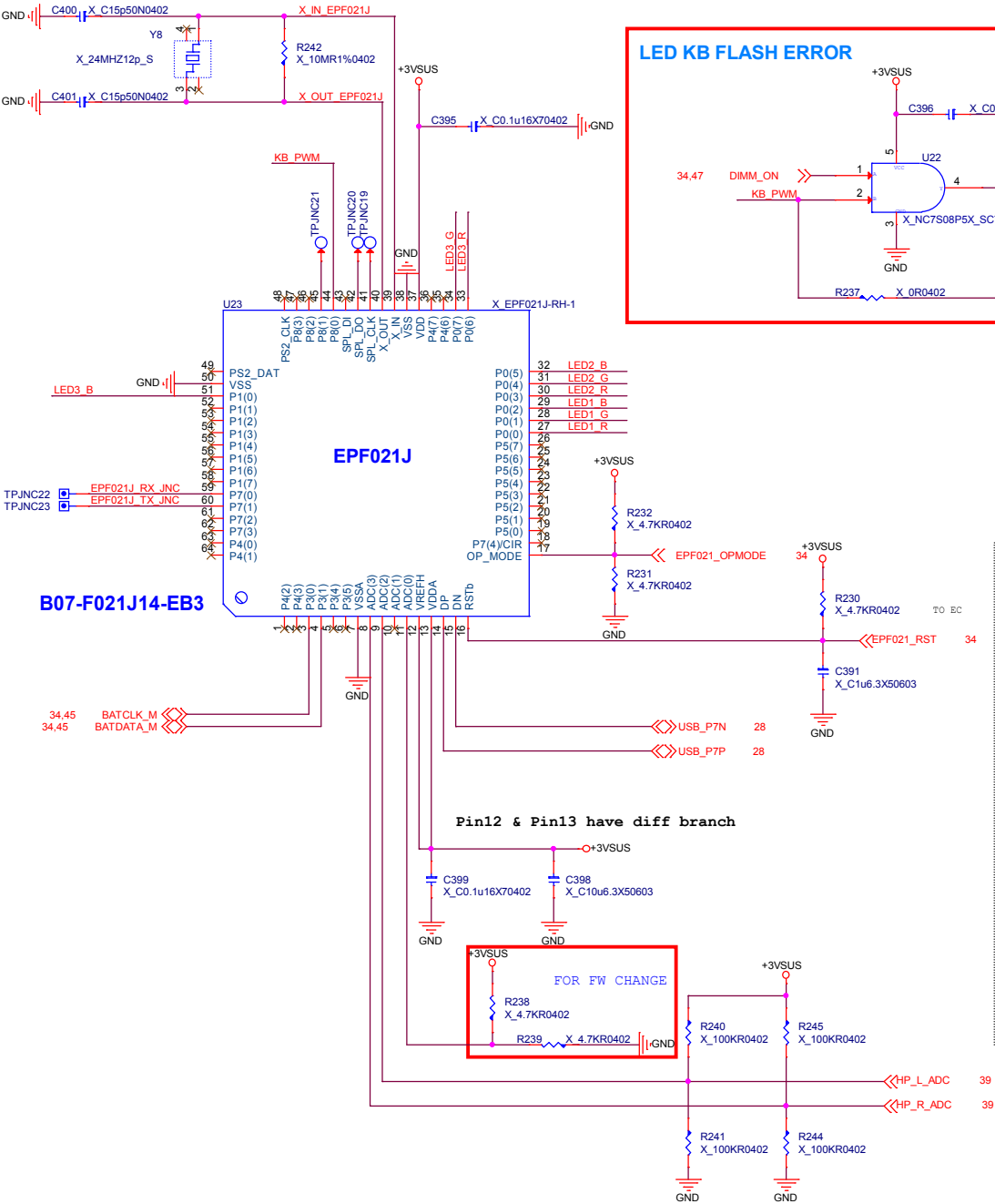


Place Close eDP Connector

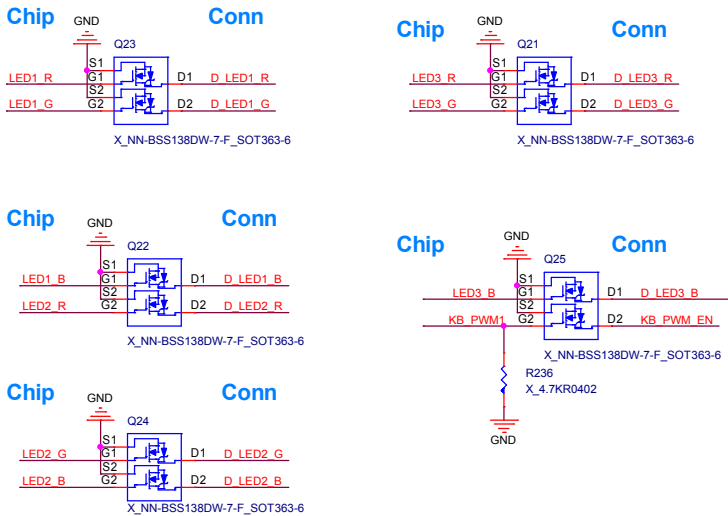
Reserve for EMI

LED 8051 Controller

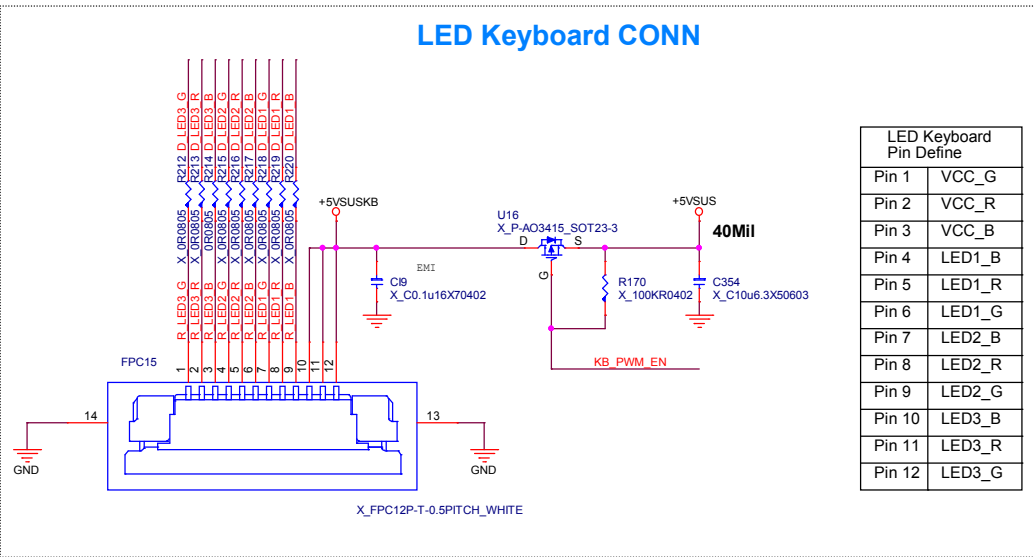
C749 and C750 change to 15pF for SA



EPF021J Sink current not enough, only using BSS138 (0.22A)



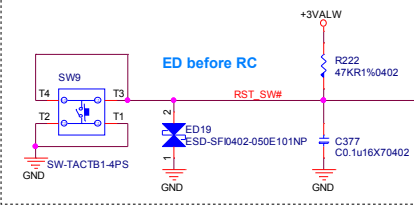
LED Keyboard CONN



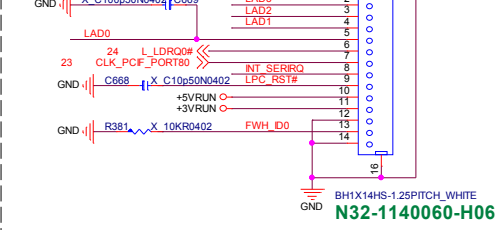
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

KBC(KB3930QFB1)

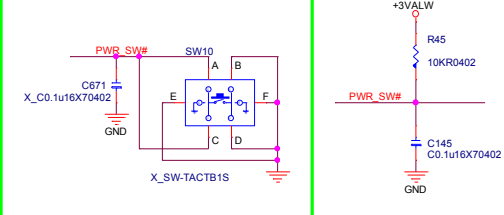
Hardware Reset



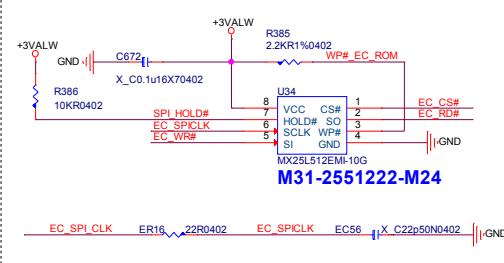
SW Debug (LPC)



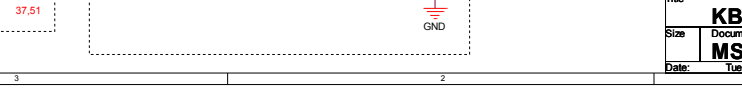
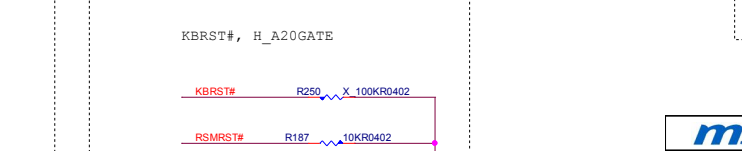
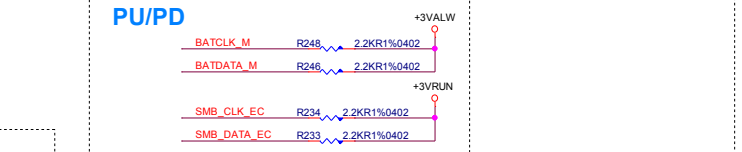
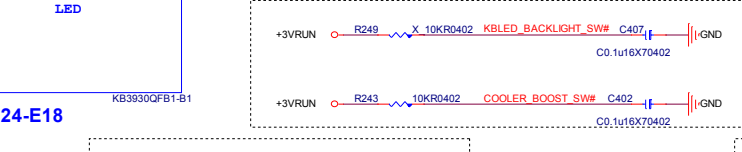
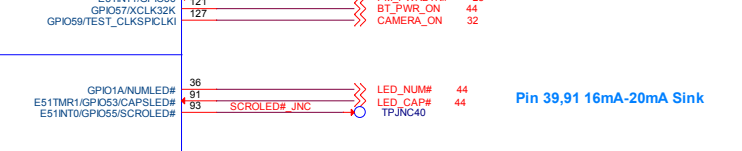
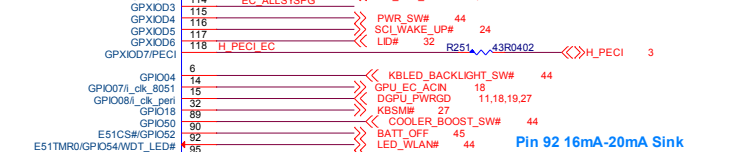
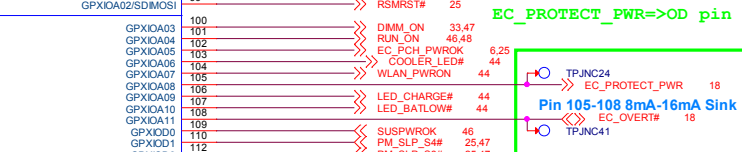
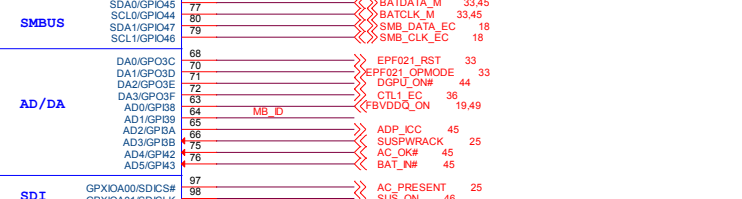
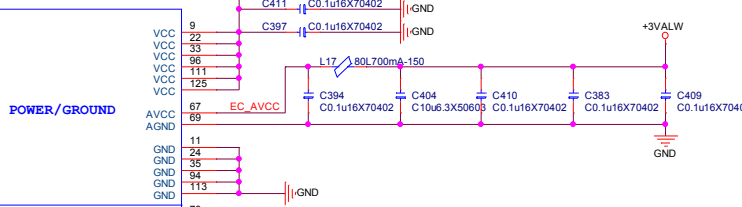
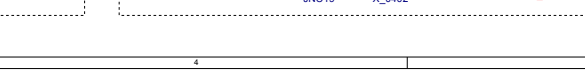
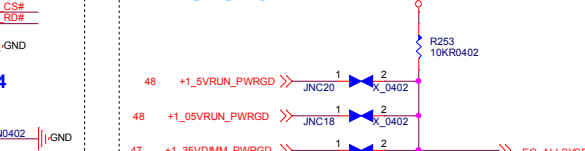
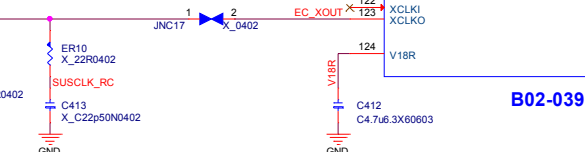
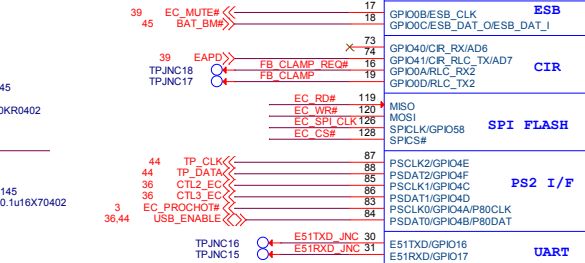
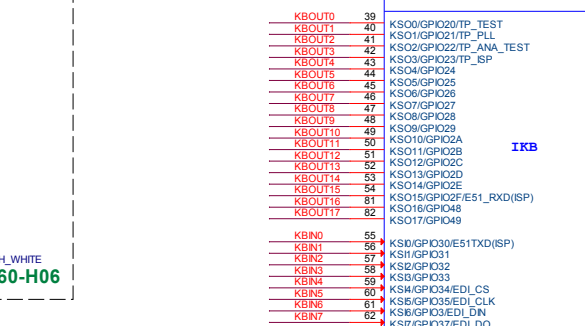
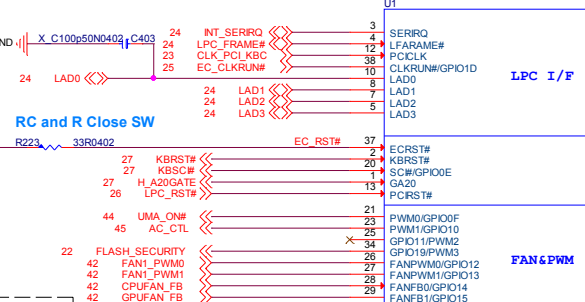
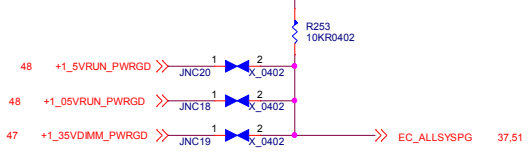
HW Debug



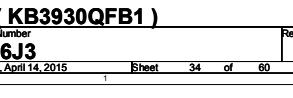
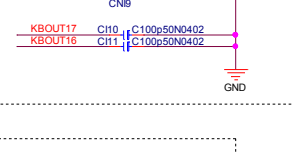
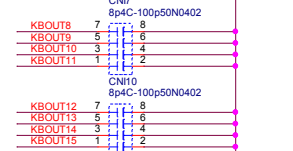
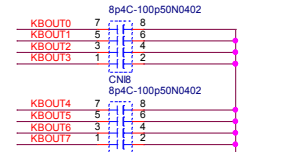
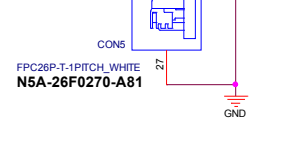
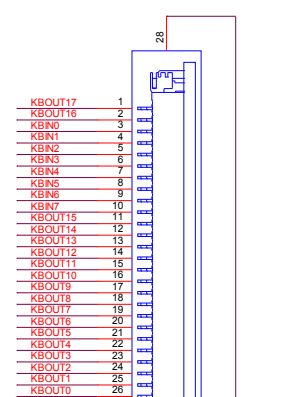
ROM

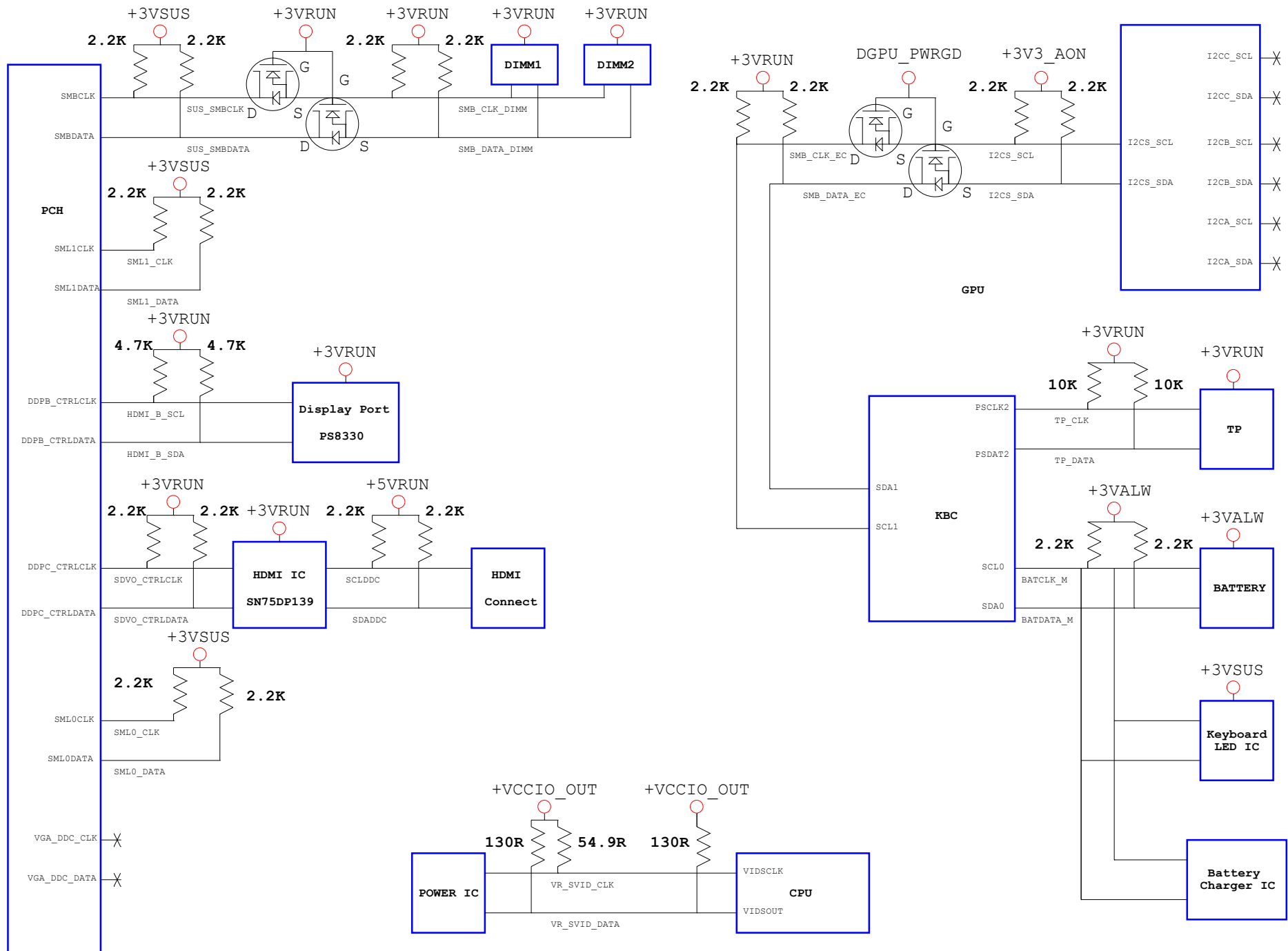


ALLSYSPG

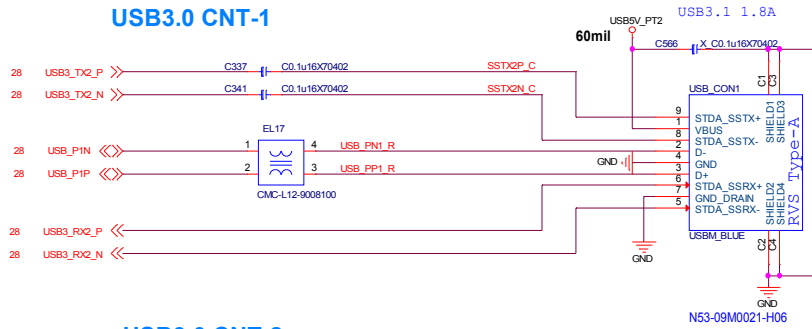


Keyboard conn

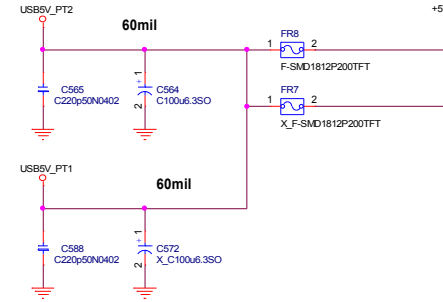
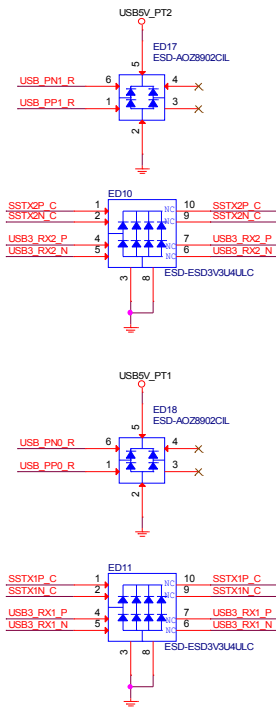
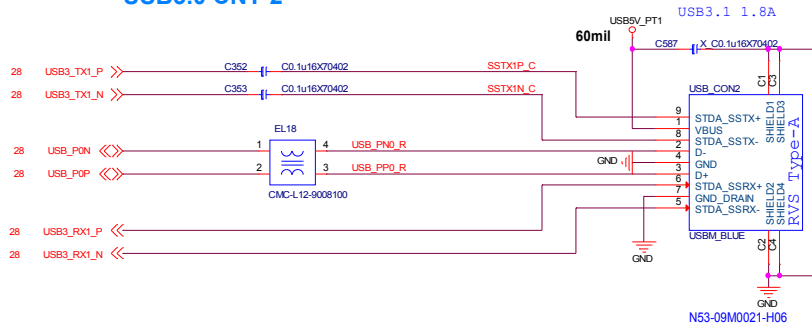




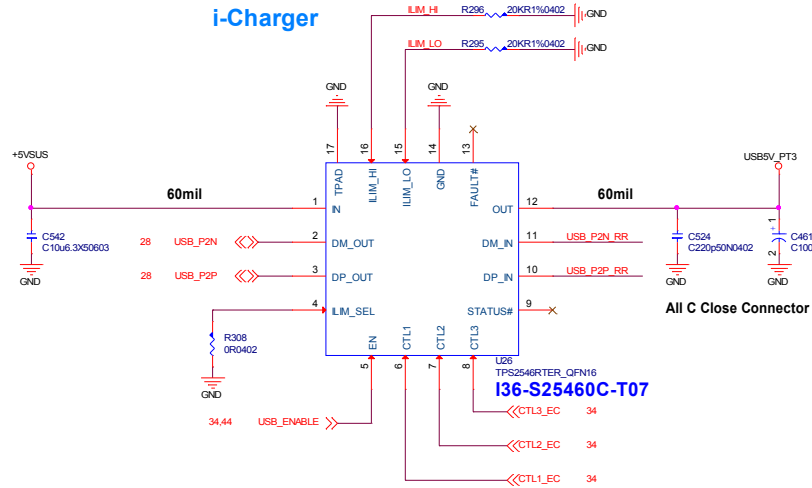
USB3.0 CNT-1



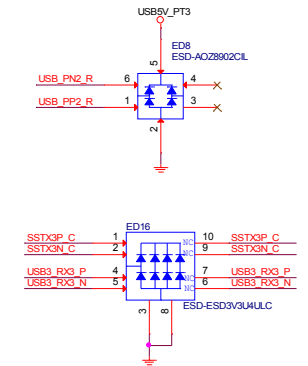
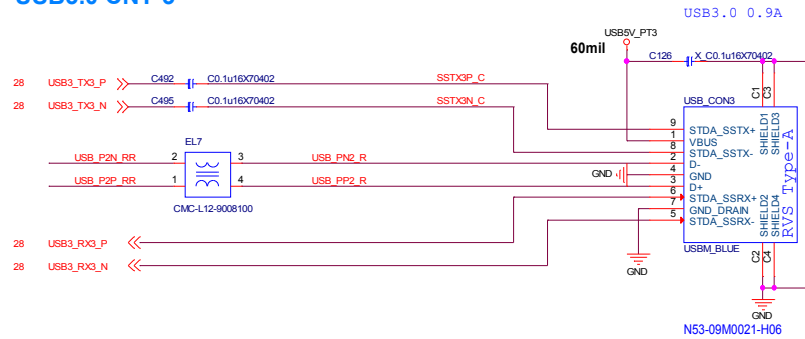
USB3.0 CNT-2



i-Charger



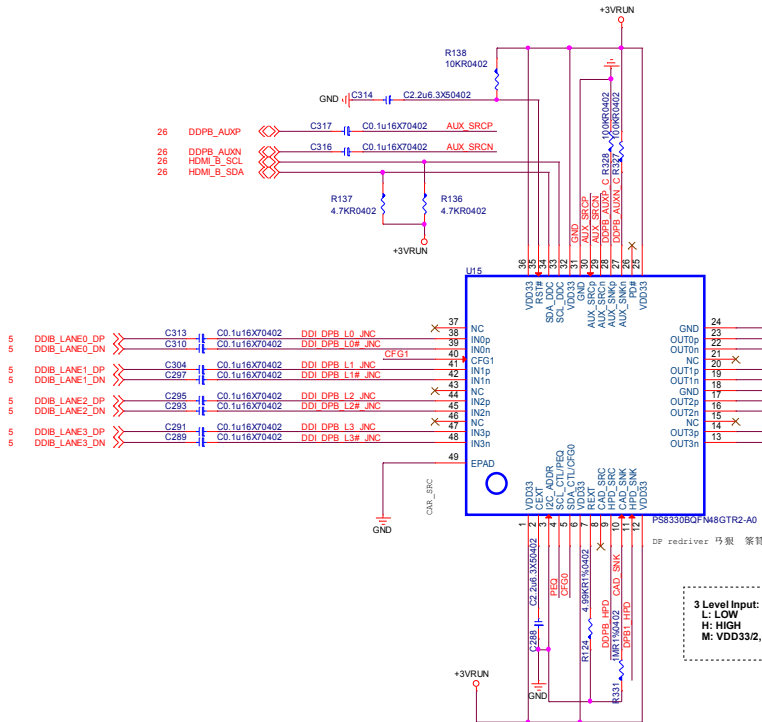
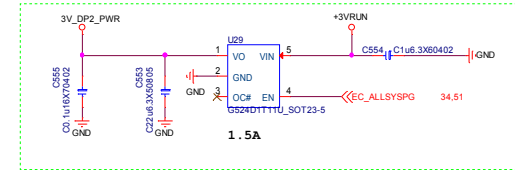
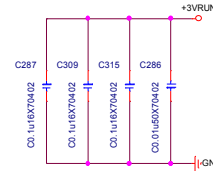
USB3.0 CNT-3



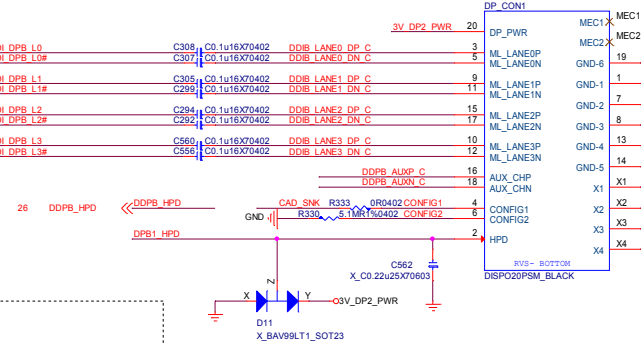
msi MICRO-STAR INT'L CO.,LTD.		
Title	USB 3.0 iCharger	
Size	Document Number	Rev
	MS-16J3	1.0
Date:	Tuesday, April 14, 2015	Sheet 36 of 60

Display Port

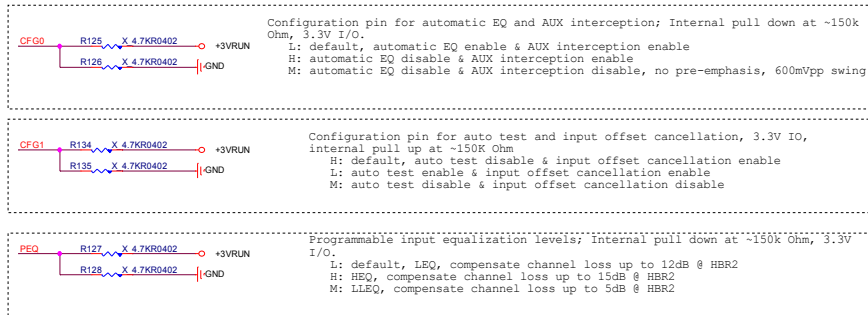
The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.



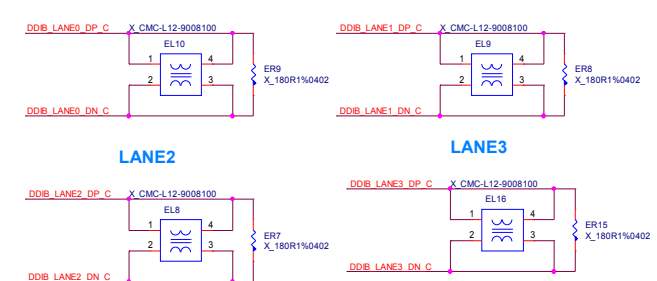
Display Port



3 Level Input:
L: LOW
H: HIGH
M: VDD33/2, connect both pull-up and pull-down resistors



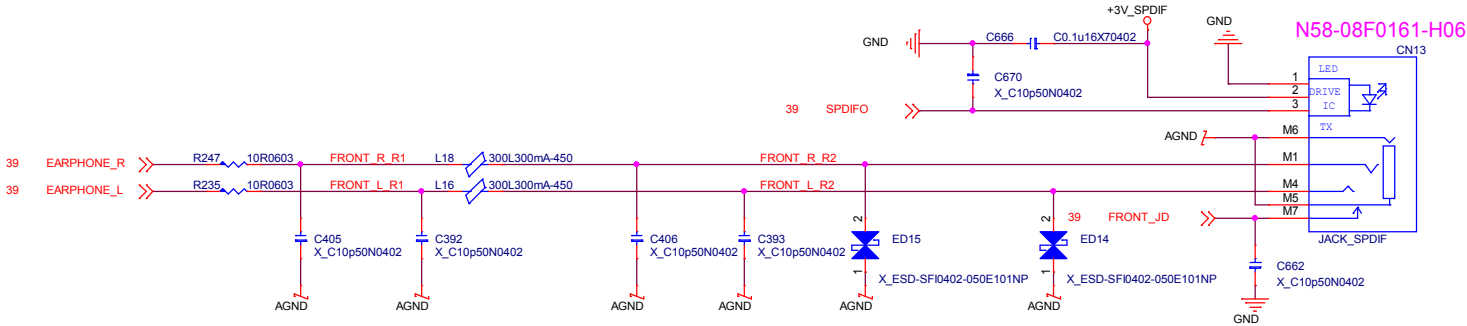
EMI Close Connector



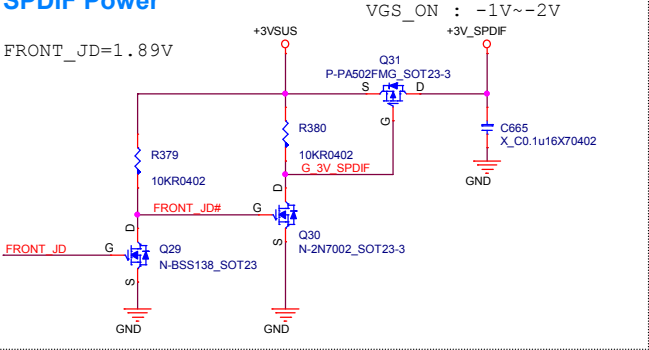
	CODEC	斥
L	-	-
L	+	+
R	+	+
R	-	-
L2	-	+
L2	+	-
R2	+	-
R2	-	+

Audio CONN / Woffler

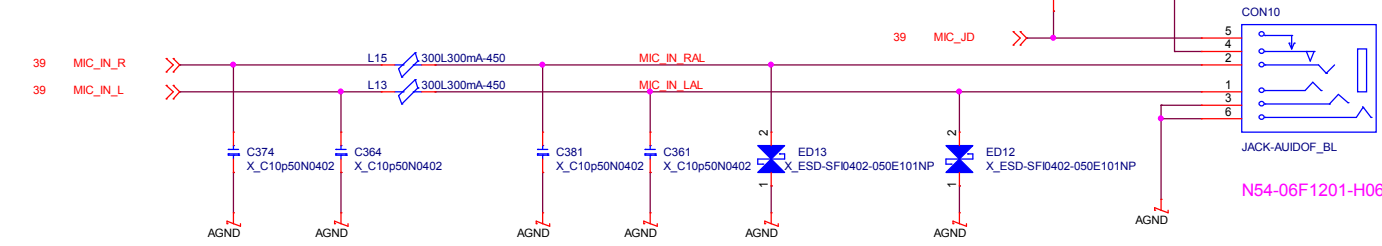
FRONT OUT



SPDIF Power



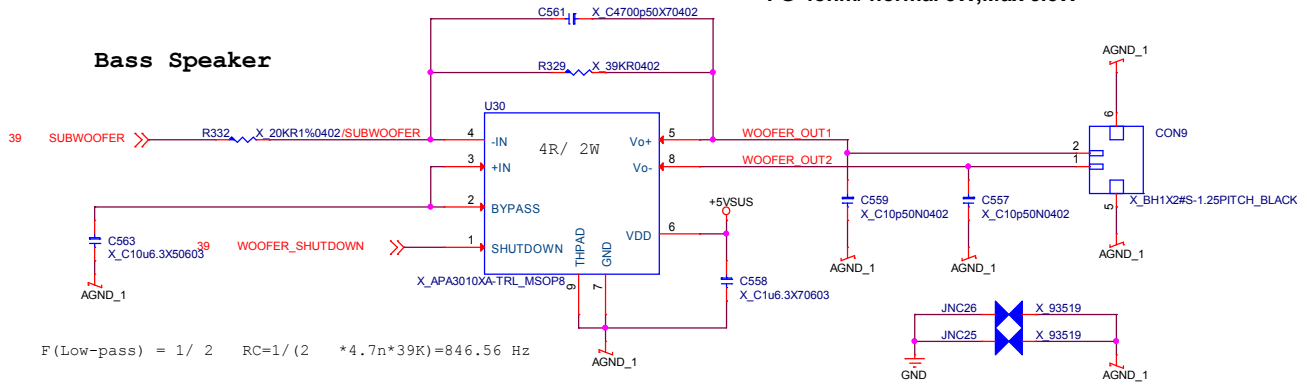
MIC IN



ALC892 SPC MAX 1.2Vrms
gain= -2*(R370/R371) = -2*(40K/20K) = -4
Vout= 0.58Vrms *4 = 2.32Vrms , Po=(2.32*2.32)/3.8=1.42W

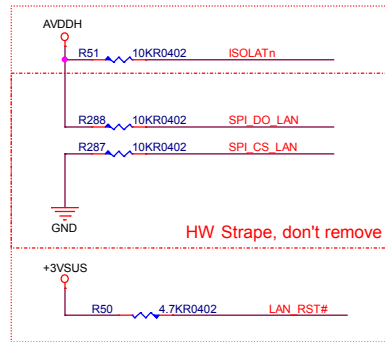
Woofer SPEC
YG 3.8ohm / normal 3W,Max 3.5W
FG 4ohm/ normal 3W,Max 3.5W

Bass Speaker

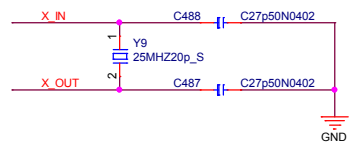


F(Low-pass) = 1/ 2 RC=1/ (2 *4.7n*39K)=846.56 Hz

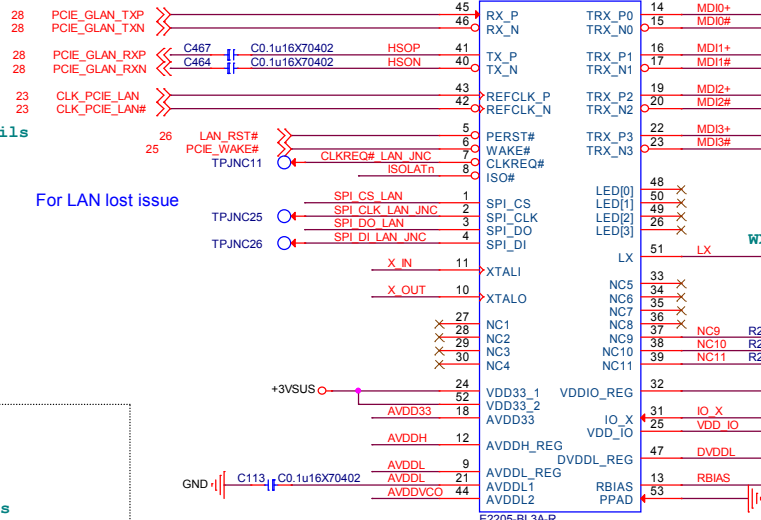
GIGA LAN(BigFoot BFN2205B)



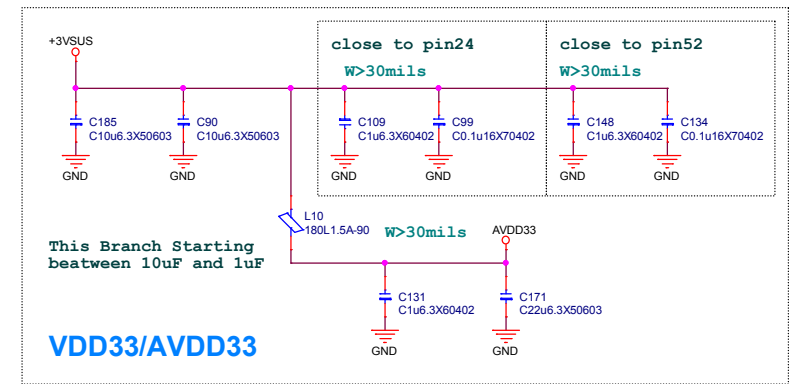
RST# spacing 20mils



For LAN lost issue

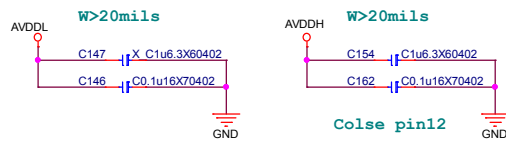


B06-E22050C-Q24

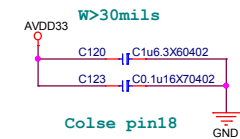


This Branch Starting
beatween 10uF and 1uF

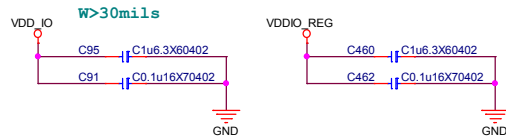
VDD33/AVDD33



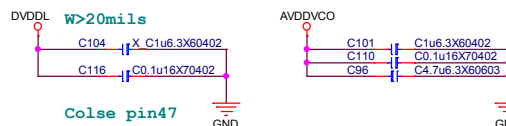
Colse pin1



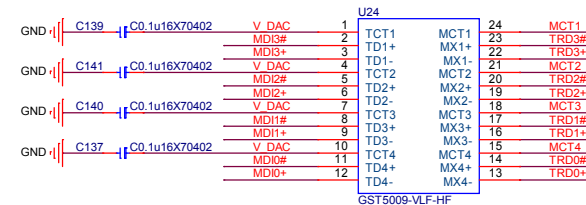
Colse pin18



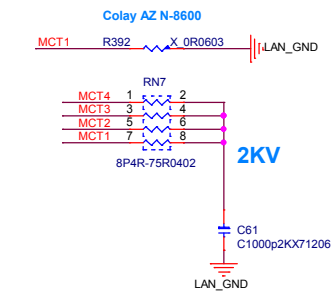
VDDIO_REG



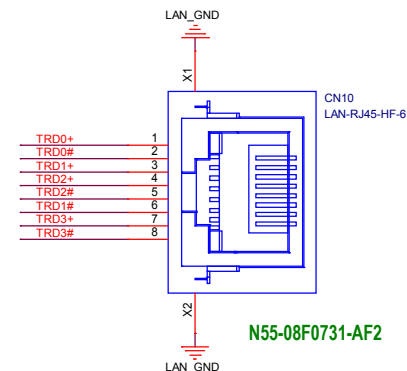
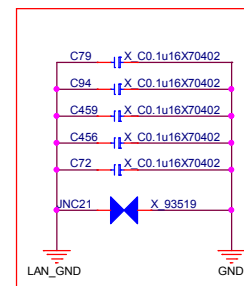
Colse pin47



L05-0200150-B09

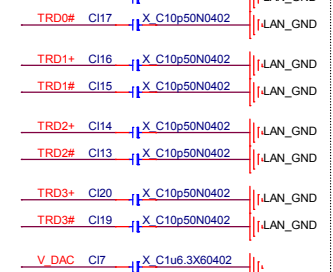


2KV

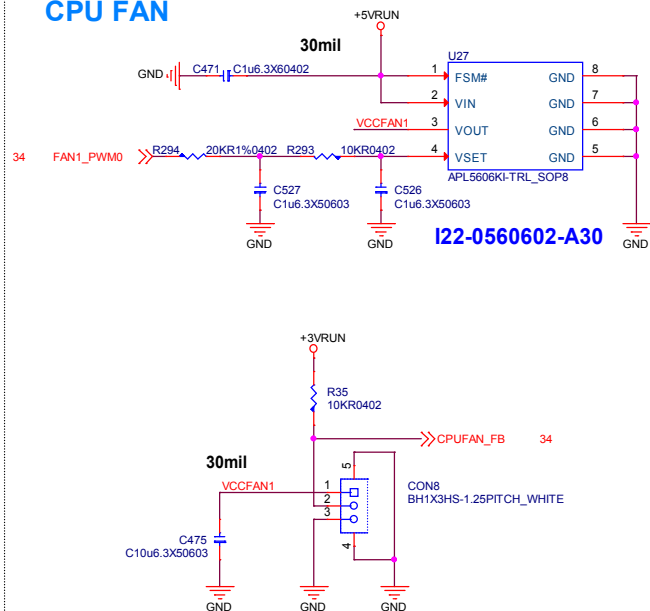


N55-08F0731-AF2

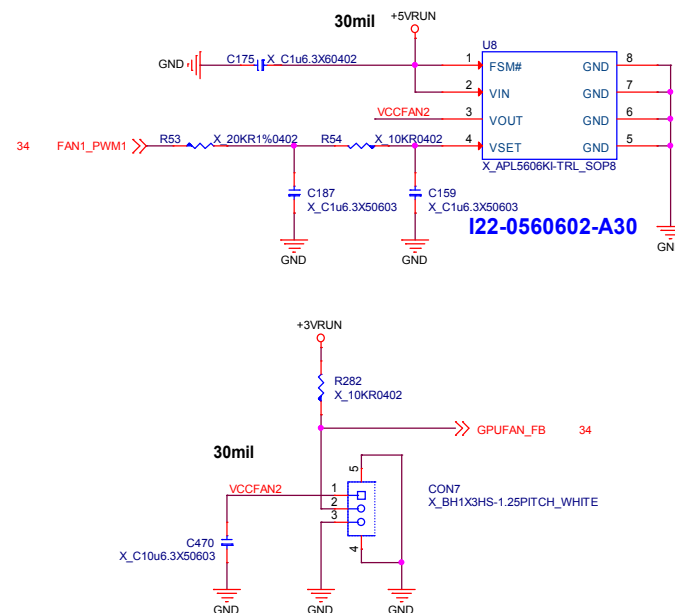
EMI



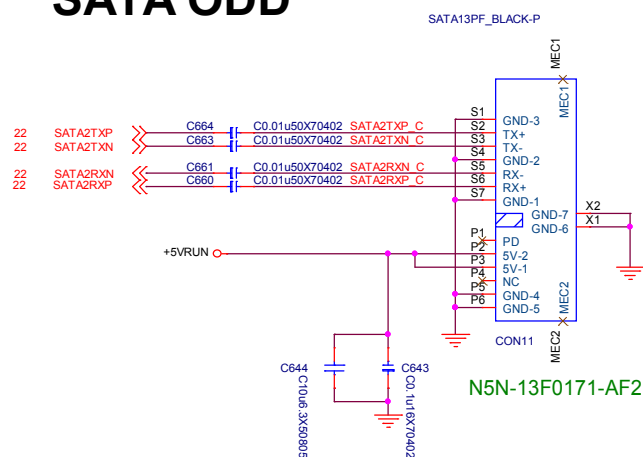
CPU FAN



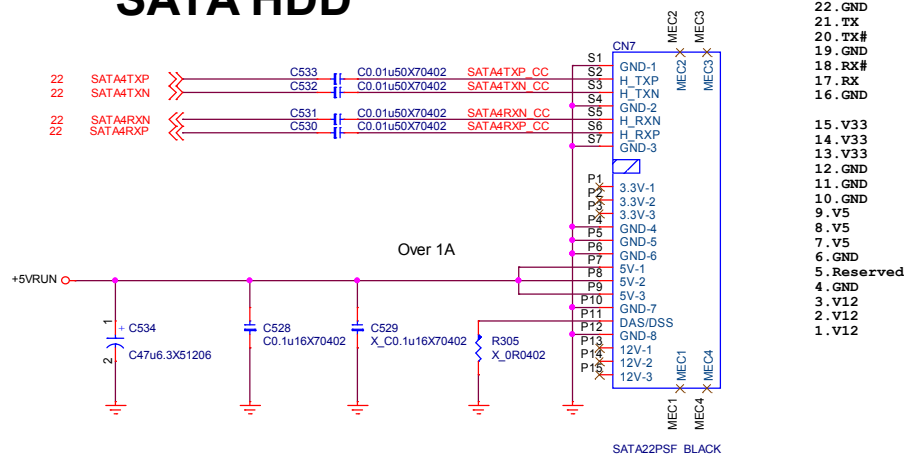
DGPU FAN



SATA ODD



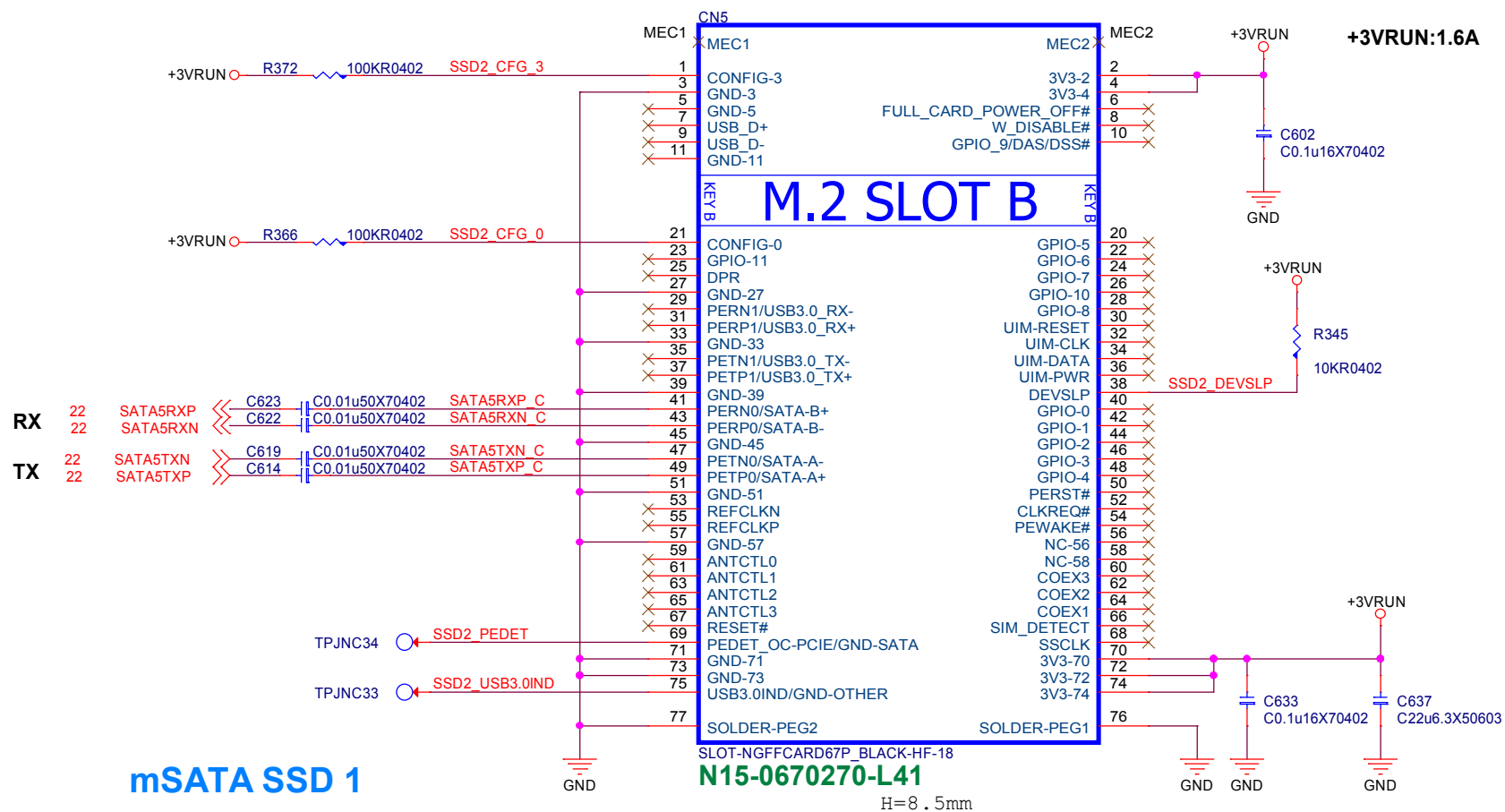
SATA HDD



22. GND
21. TX
20. TX#
19. GND
18. RX#
17. RX
16. GND

15. V33
14. V33
13. V33
12. GND
11. GND
10. GND
9. V5
8. V5
7. V5
6. GND
5. Reserved
4. GND
3. V12
2. V12
1. V12

SSD

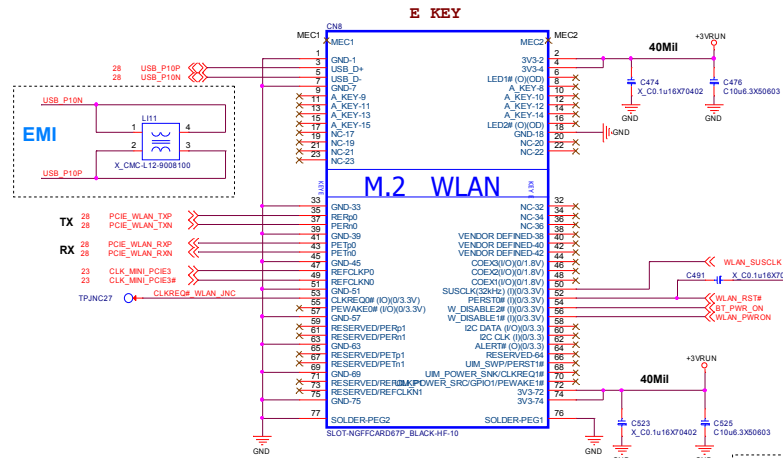


mSATA SSD 1

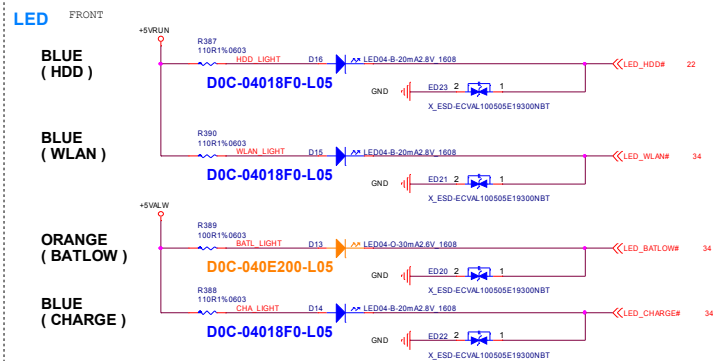
N15-0670270-L41

H=8.5mm

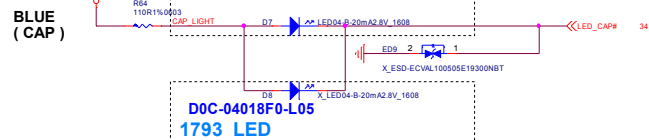
WLAN/LED



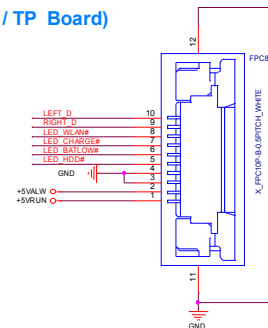
16J3 LED



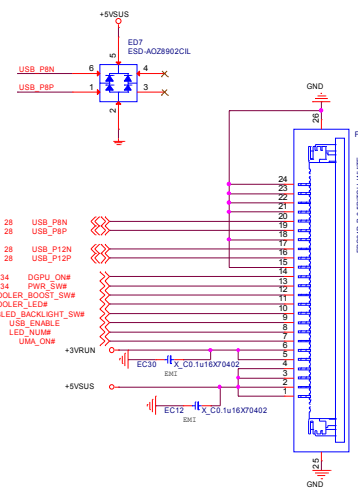
16J3 LED



To 1793B (LED / TP Board)

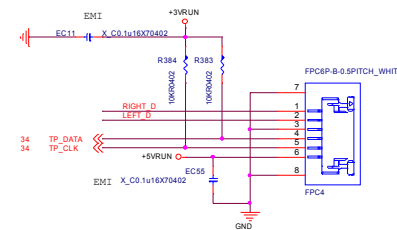


To 16J12 (Power Board/USB2.0/Card Reader Board)

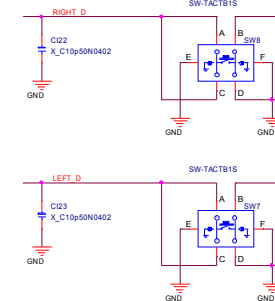


Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

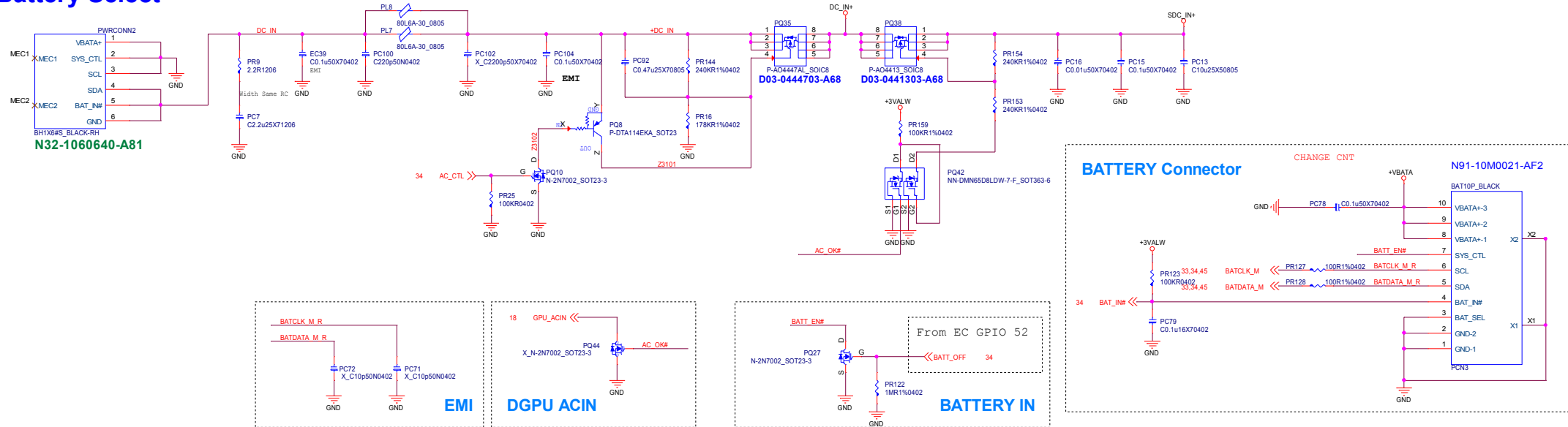
Touch Pad



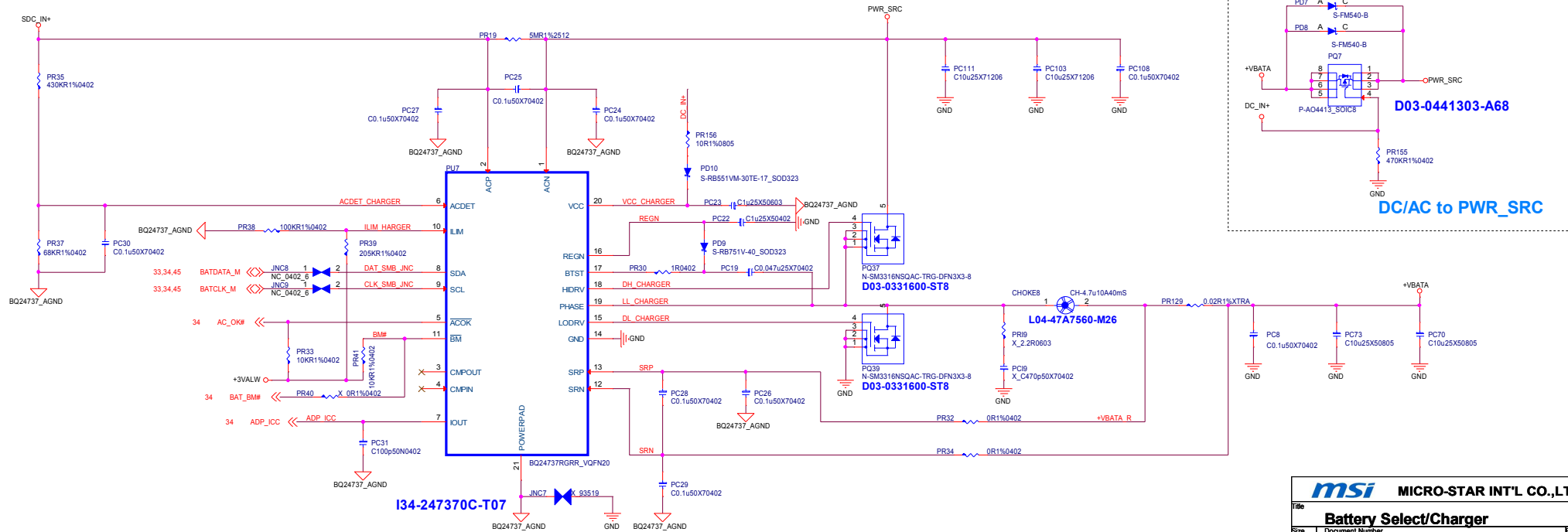
16J3 Touch Pad Switch



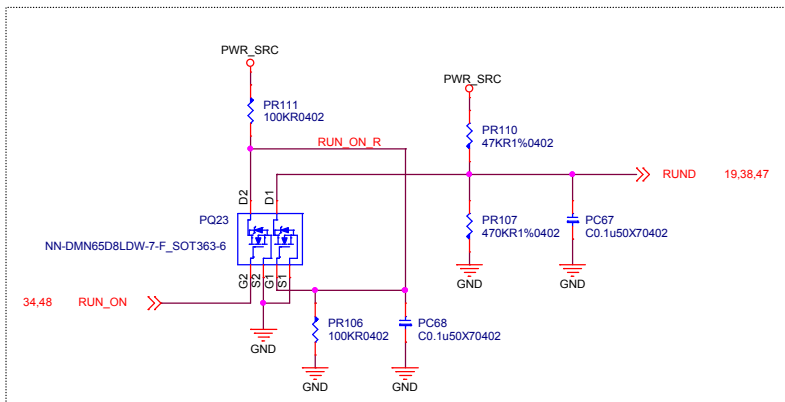
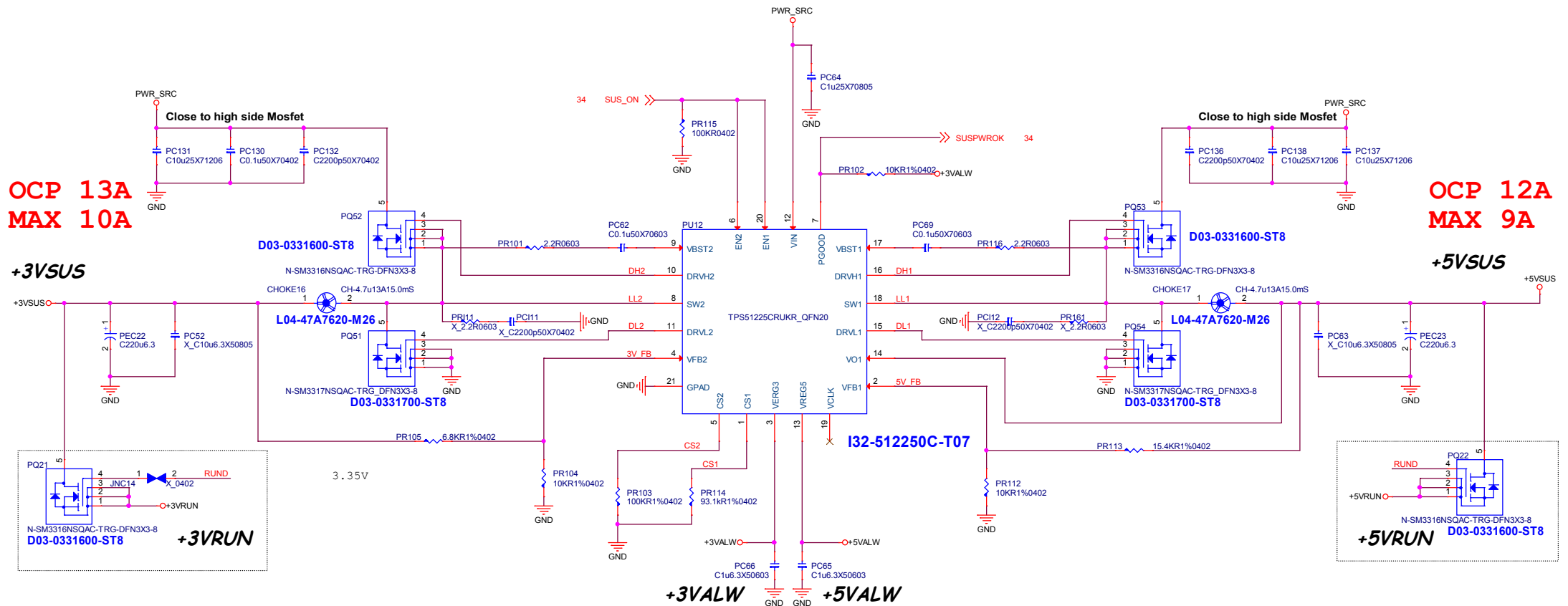
Battery Select



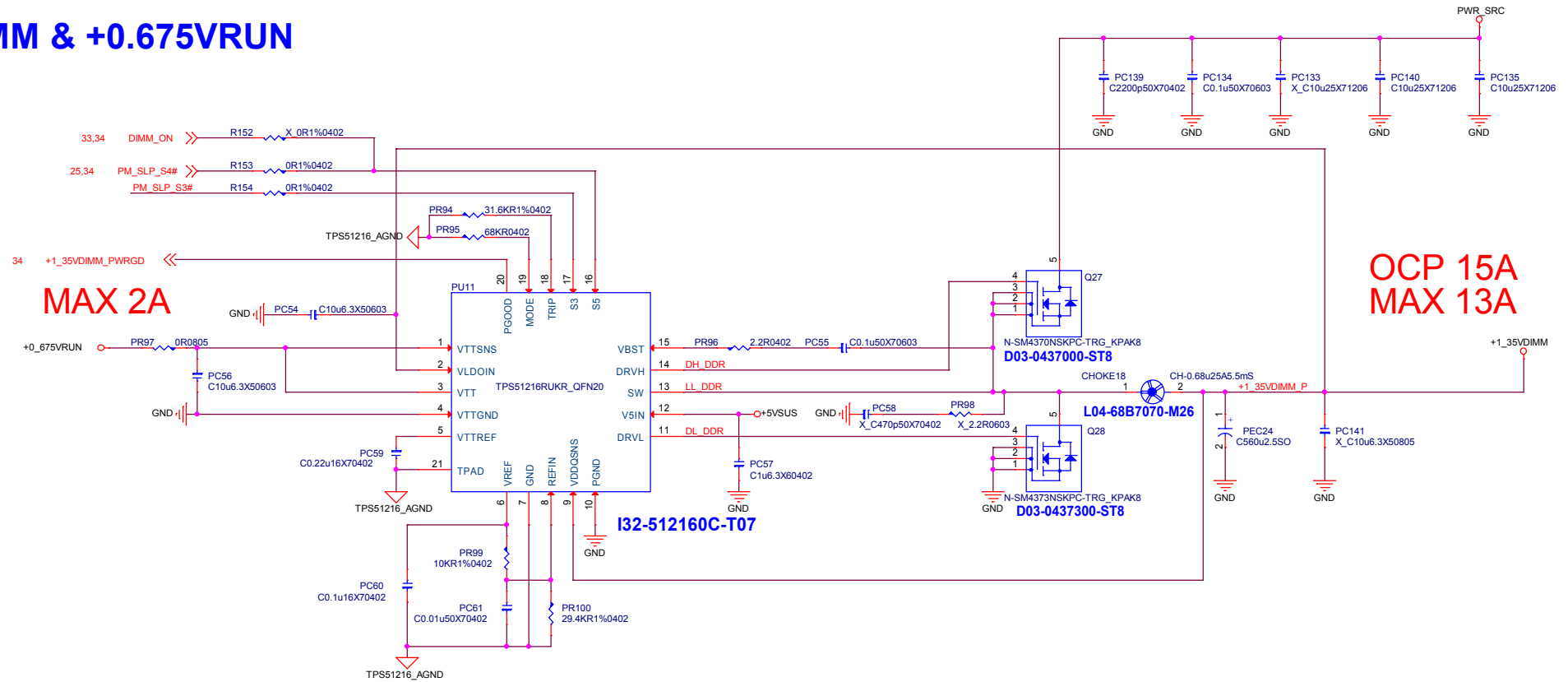
Battery Charger



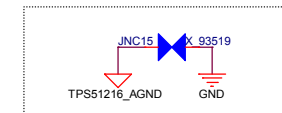
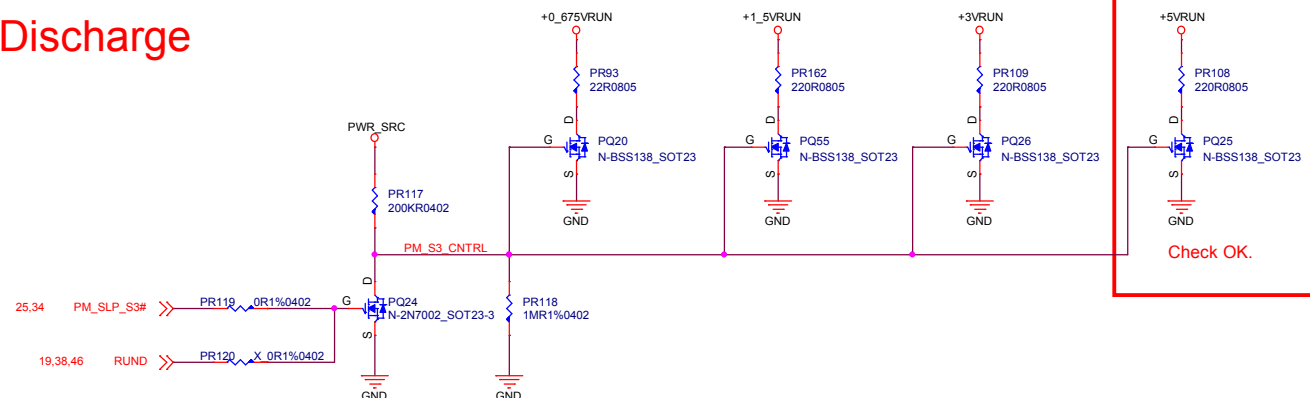
System Power



+1.35VDIMM & +0.675VRUN



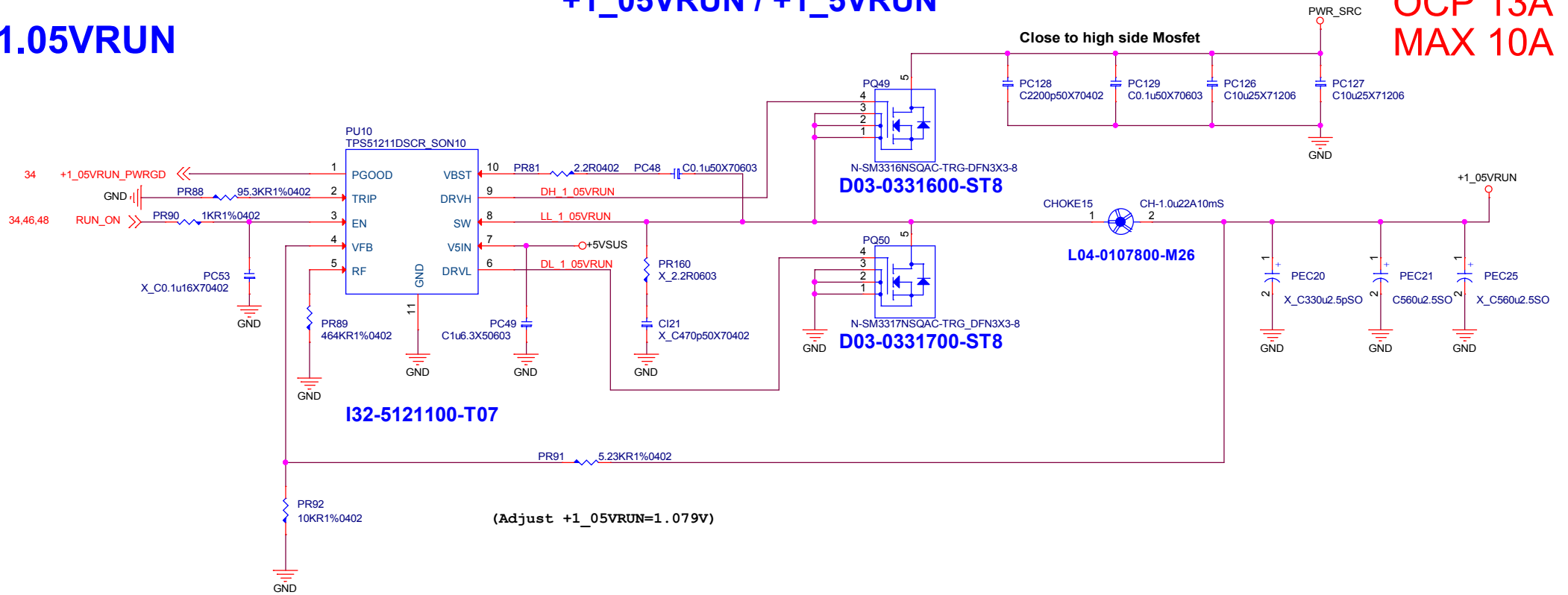
Discharge



+1.05VRUN

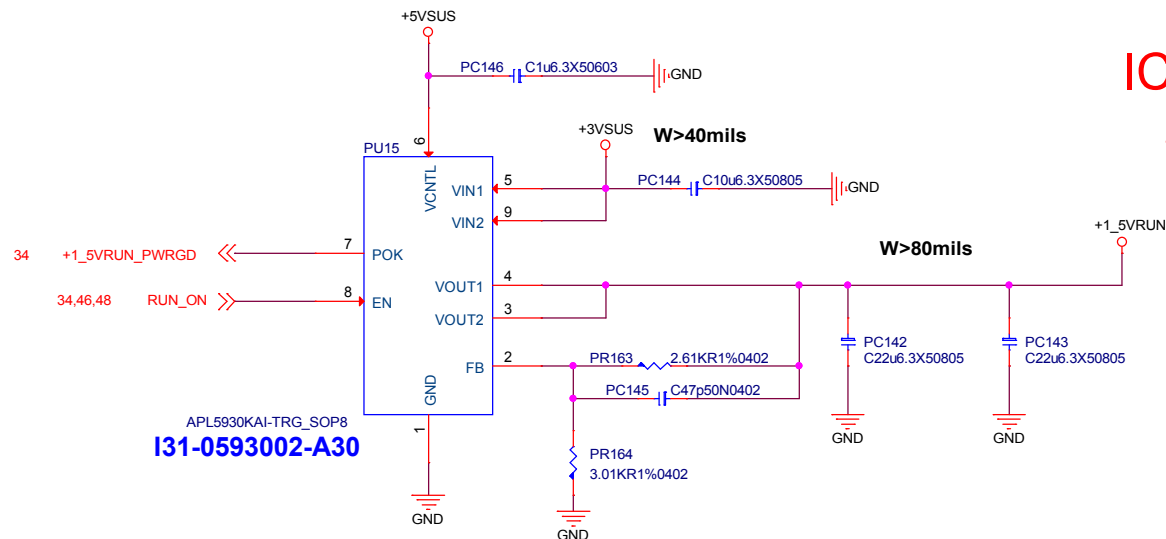
+1_05VRUN / +1_5VRUN

OCP 13A
MAX 10A



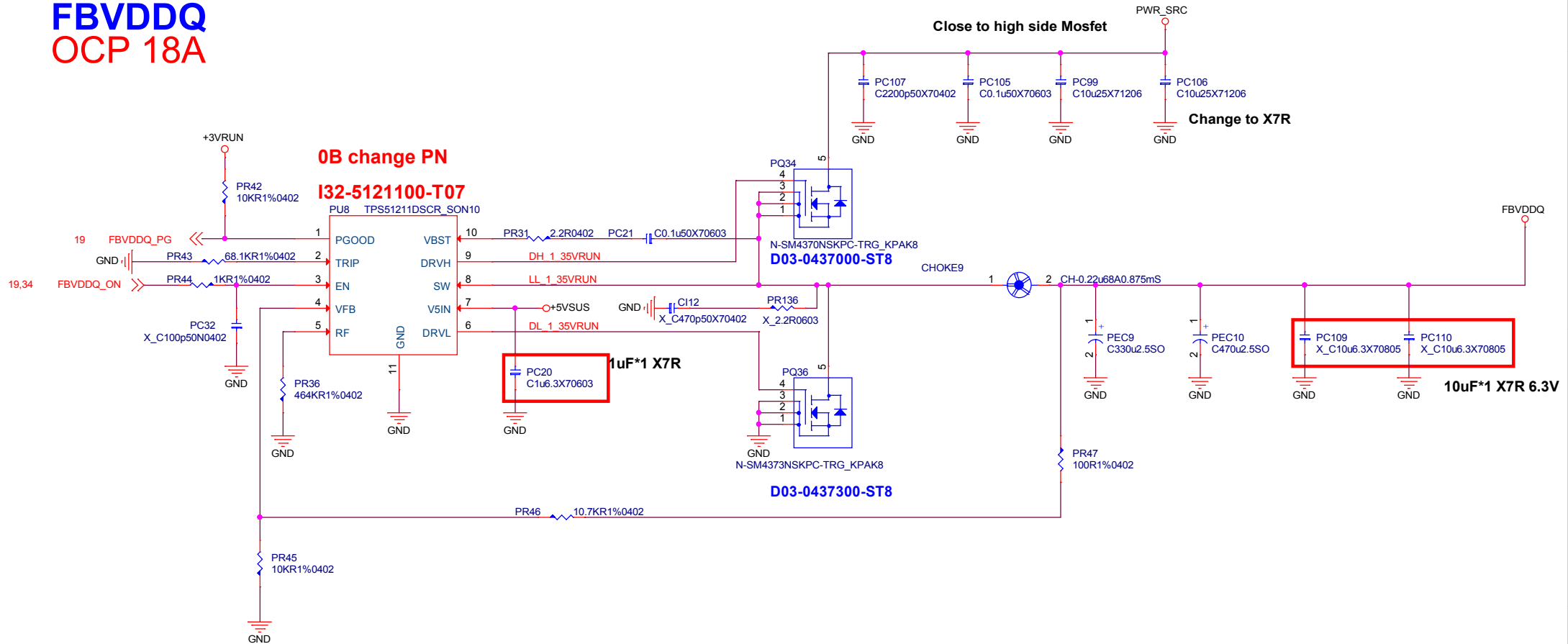
+1.5VRUN

IC MAX 3A
253mA



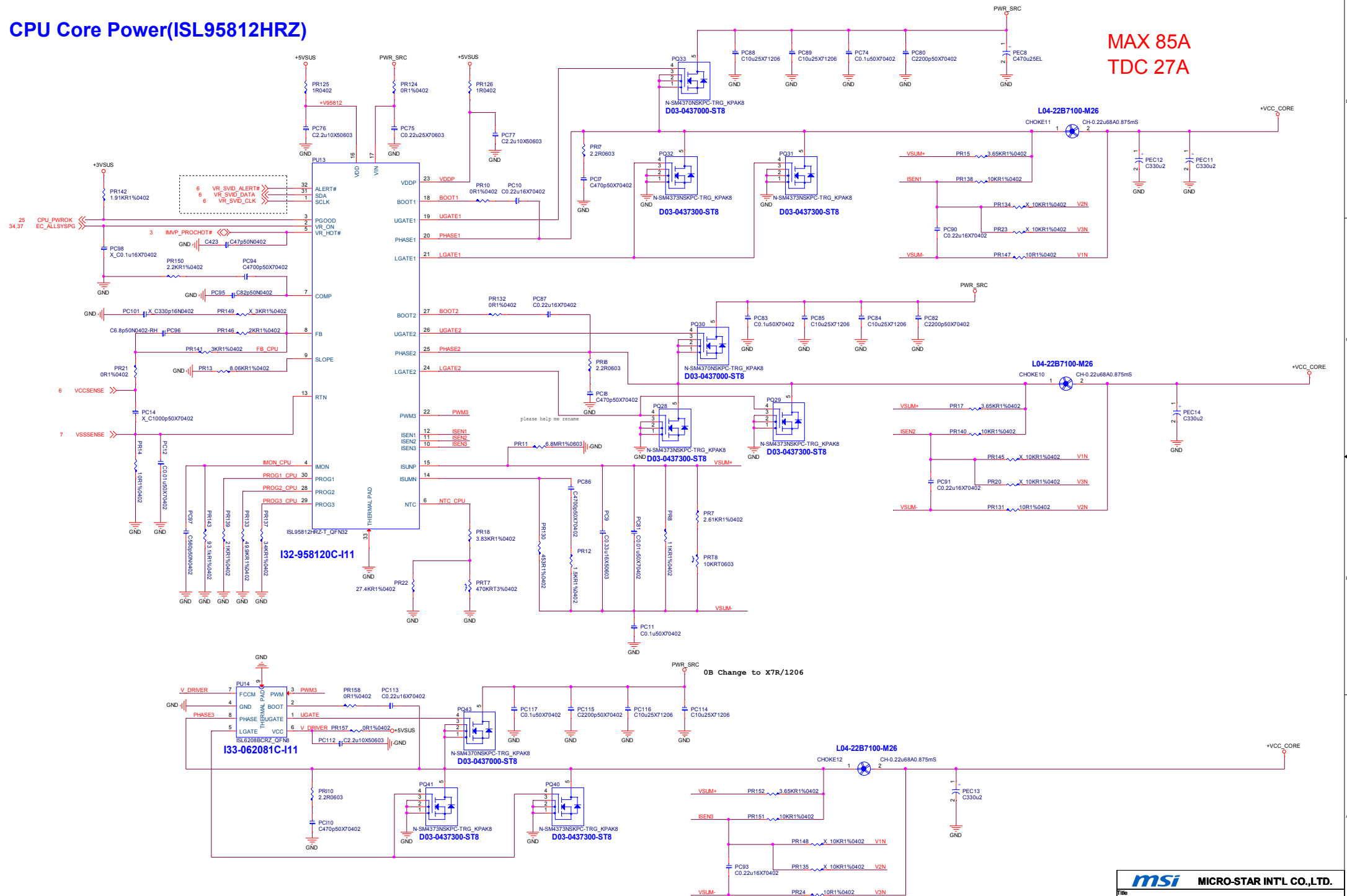
DGPU POWER FBVDDQ

FBVDDQ
OCP 18A

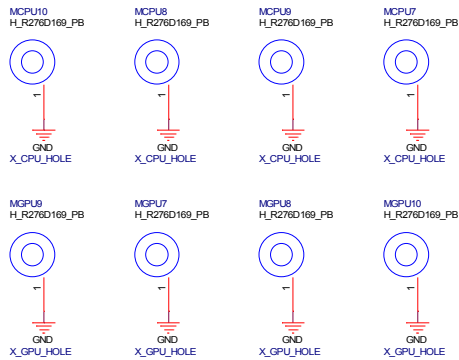


CPU Core Power(ISL95812HRZ)

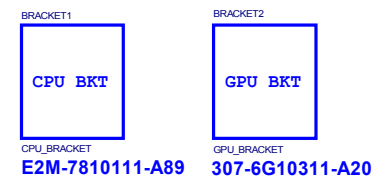
MAX 85A
TDC 27A



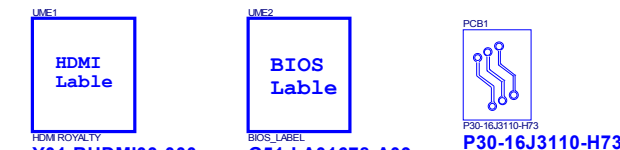
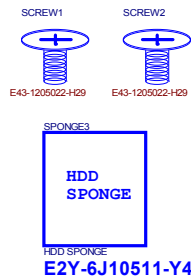
CPU/GPU Holes



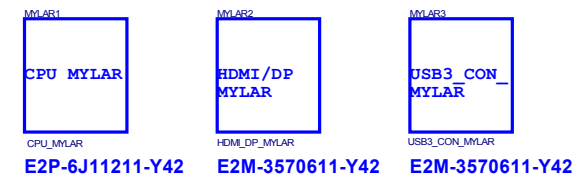
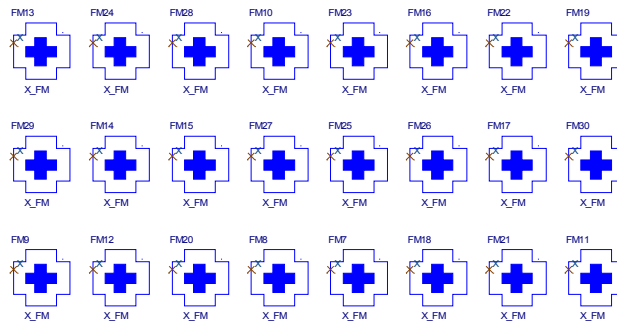
CPU/GPU BRACKET



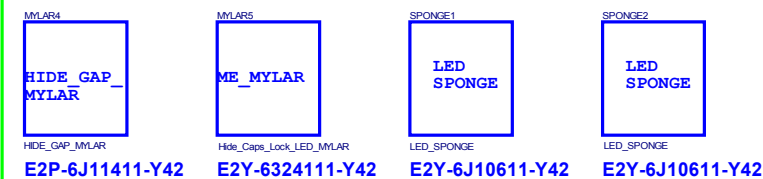
HDD



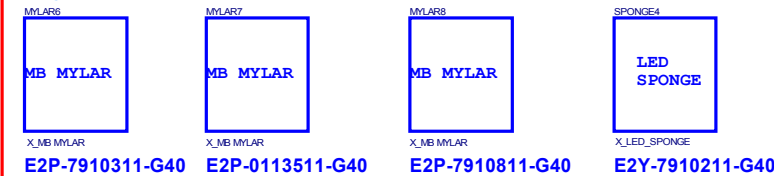
Hannstar: P30-16J3110-H73
TRIPD: P30-16J3110-T53



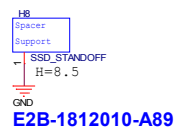
Only 16J3



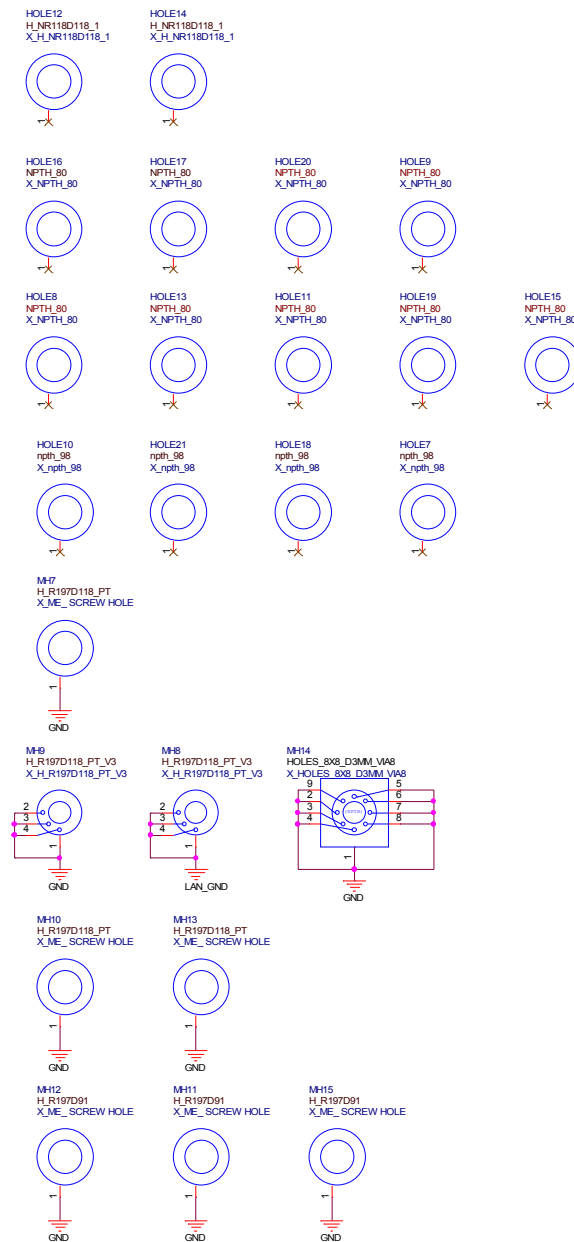
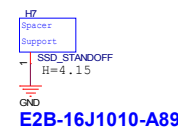
Only 1793



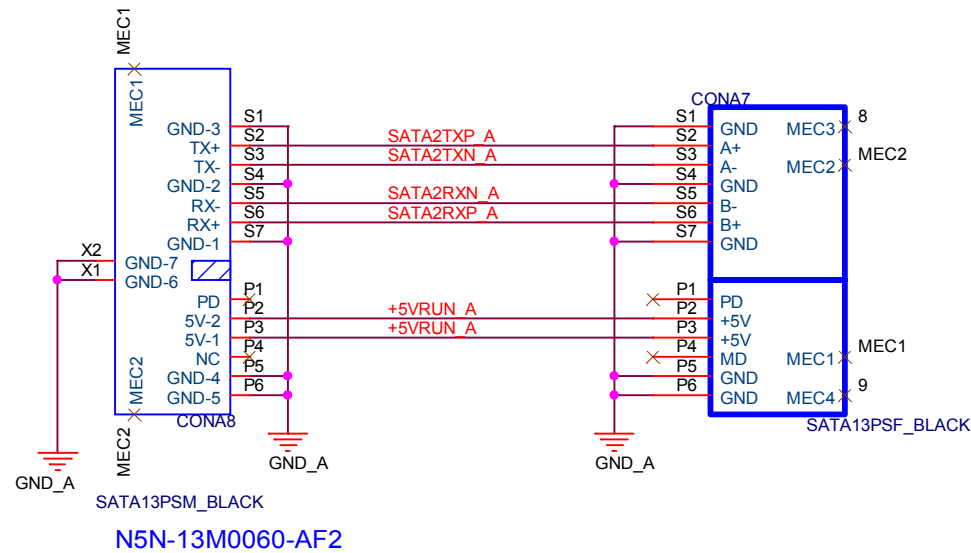
mSATA SSD 1 STAND OFF



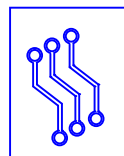
WLAN STAND OFF



1793-A Board (ODD)



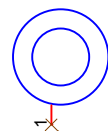
PCBA1



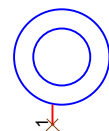
P30-16J3A10-H73

P30-16J3A10-H73

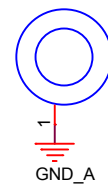
HB10
NPTH_80
X_NPTH_80



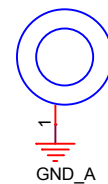
HB7
NPTH_80
X_NPTH_80



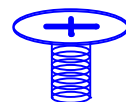
MB7
H_R197D91
X_H_R197D91



MB8
H_R197D91
X_H_R197D91

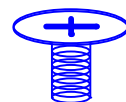


SCREWA2



E43-1205003-H29

SCREWA1



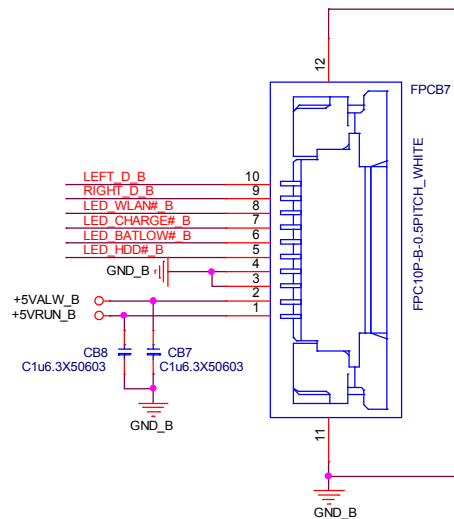
E43-1205003-H29



MICRO-STAR INT'L CO.,LTD.

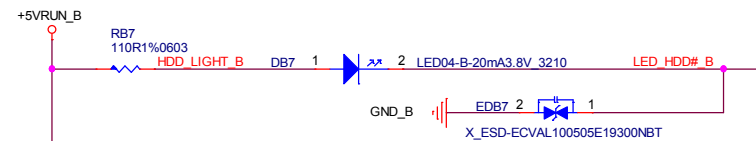
Title		
[A] 1793 ODD		
Size	Document Number	Rev
A4	MS-16J3	1.0
Date:	Tuesday, April 14, 2015	Sheet 54 of 60

1793-B Board (LED / TP)

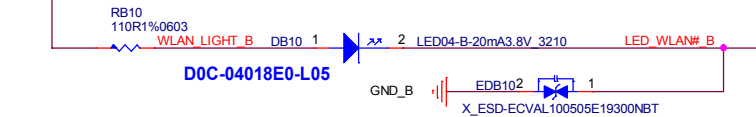


LED FRONT

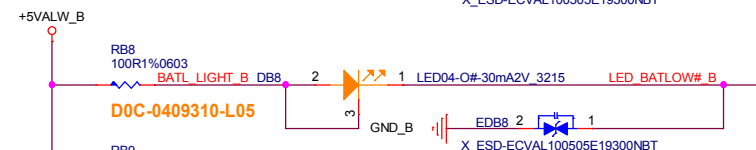
BLUE
(HDD)



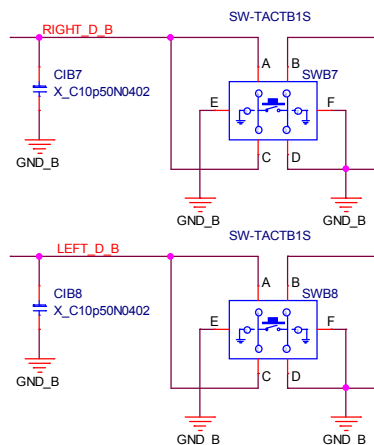
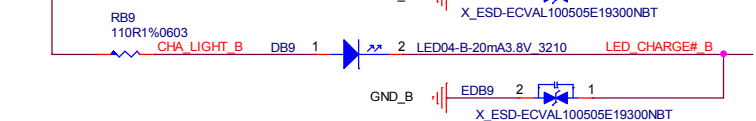
BLUE
(WLAN)



ORANGE
(BATLOW)

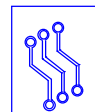


BLUE
(CHARGE)



H=1.5mm

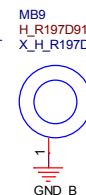
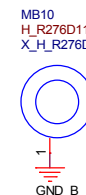
PCBB1



P30-16J3B10-H73

P30-16J3B10-H73

Hannstar: P30-16J3B10-H73
 TRIPOD: P30-16J3B10-T53



msi

MICRO-STAR INT'L CO.,LTD.

Title

[B] 1793 LED / TP

Size

Document Number

MS-16J3

Rev

1.0

Date:

Tuesday, April 14, 2015

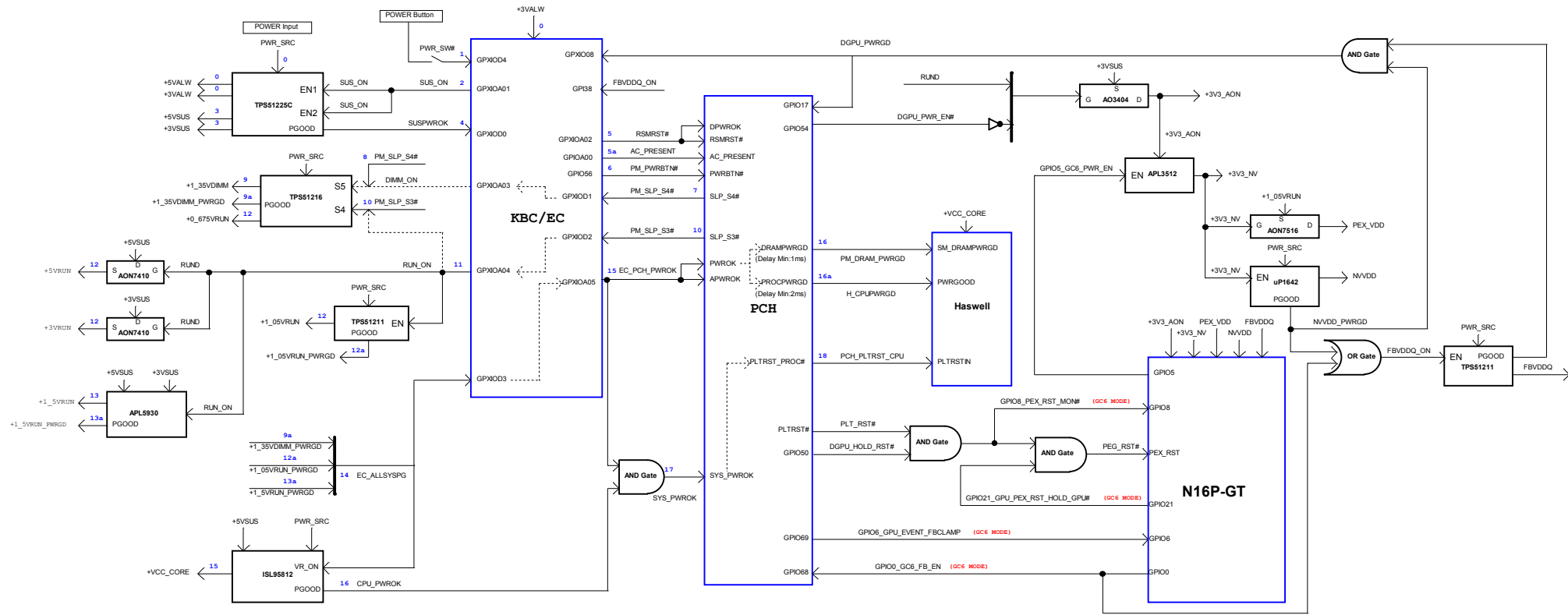
Sheet

55

of

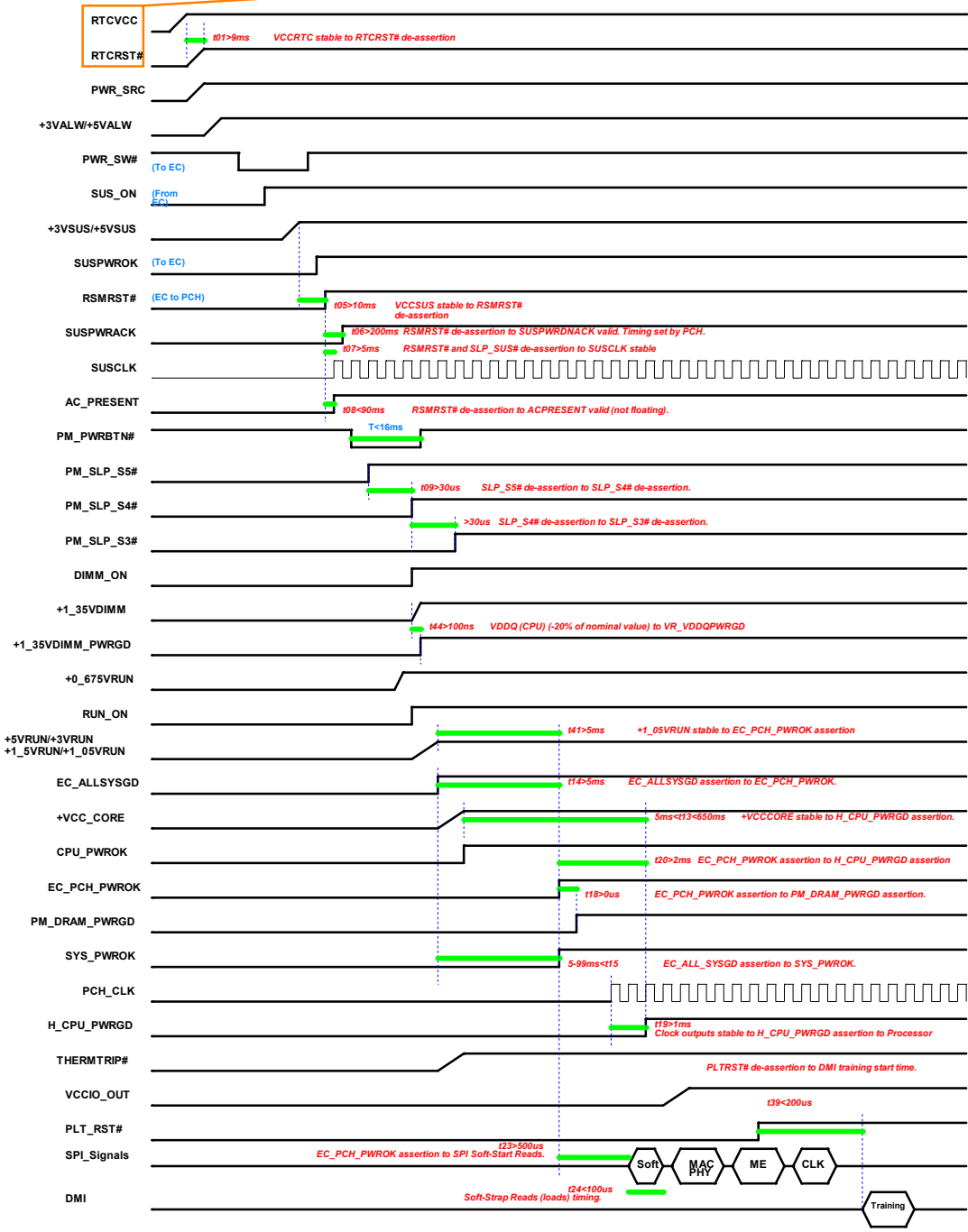
60

MS-16J3 Power on Block Diagram

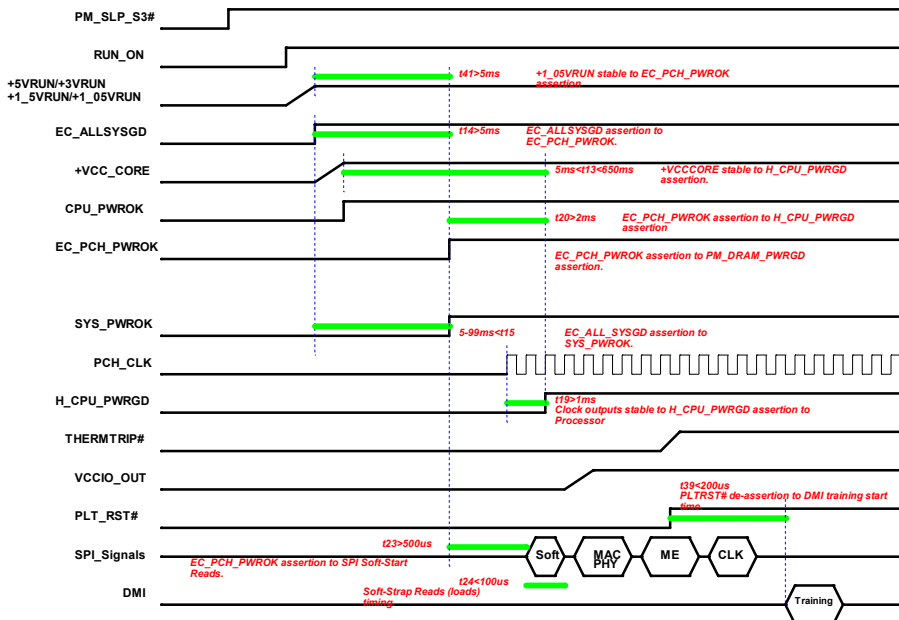


Power on Sequence

G3 -> S0

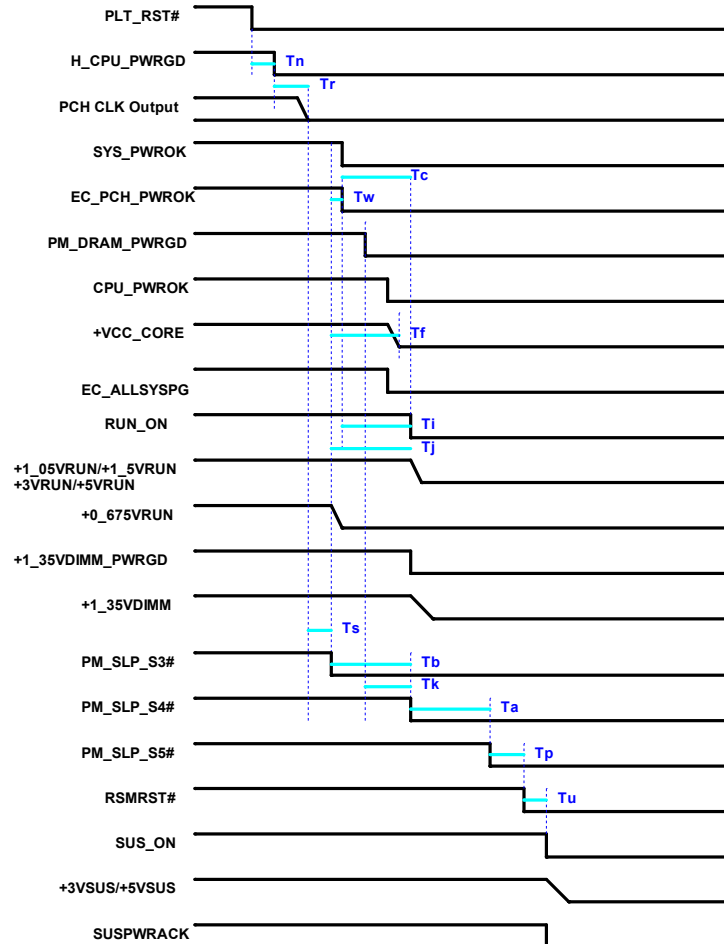


S3-> S0



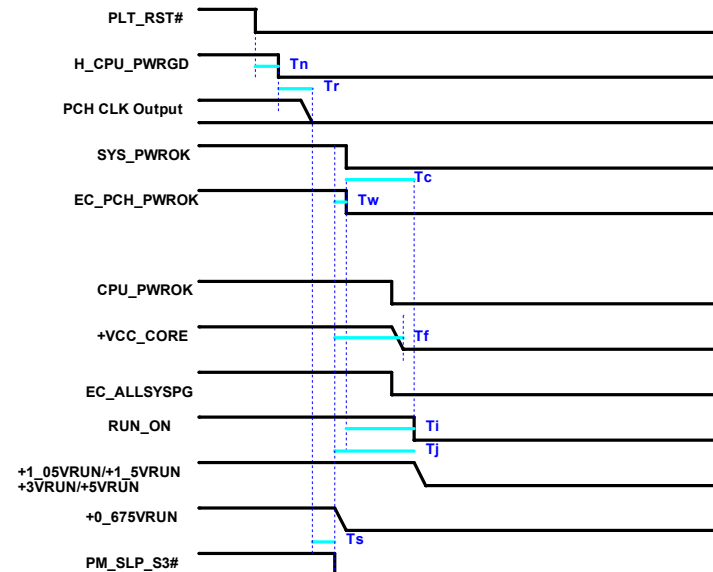
Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

S0 -> S3



History

0A: 2014/12/24

- 01. P05 DEL TPJNC5
DEL TPJNC4
ADD R62 TO U68 PIN AB49
ADD R63 TO U68 PIN V51
- 02. P26 ADD R293 TO DGPU_PWR_EN#
ADD U18 R292 C495
- 03. P27 DEL R121
DEL R204

2014/12/28

- 01. P05 CON3 N32-10200Q0-A81 change N91-02F0080-H06
BAT1 D06-0105701-K26 change D06-0100101-K26
- 02. P36 DEL U29 U27 C669 C689
ADD FR1 FR2
C670 C71-101064G-S03 change C71-2210630-S03
C687 C71-101064G-S03 change C71-2210630-S03
ADD ED11 ED12 ED13 ED14 ED16
- 03. P44 ADD ED17

2014/12/29

- 01. P22 DEL SATA1TXP SATA1TXN SATA1RXP SATA1RXN
DEL SATA0TXP SATA0TXN SATA0RXP SATA0RXN
- 02. P26 DEL R284
- 03. P28 DEL C437 C438 C436 C435 C433 C434
DEL C432 C429 C427 C428
- 04. P35 DEL C42 C379 C381 C386 C387 C388 C389 C394 C401 C402
C410 C412 C413 C414 C415 C416 C431 C673 C674 C675
C675 C676 C677 C678 C679 C680 C682 C683 C684 C685
C686
DEL R151 R152 R154 R165 R167 R168 R169 R170 R173 R174
R181 R182 R183 R186 R187 R189 R196 R201 R202 R209
R210 R212 R217 R218
DEL TPJNC8 TPJNC9 TPJNC10 TPJNC11
DEL U9 U10 U11 Y1 CHOKE2
- 05. P36 DEL R178 R180 R397 R399 R172 R176
DEL R177 R179 R398 R400 R171 R175
DEL R185 R195 R408 R411 R198 R200
DEL R184 R194 R409 R412 R197 R199
- 06. P38 ADD Q5 R86 C151
- 07. P43 DEL C472 C473 C476 C801 C802 C803 C804
DEL R283 R475 R476
DEL TPJNC41 TPJNC42
DEL CN4
DEL C461 C462 C463 C768 C777 C779 C788 EC41 EC42
DEL R262 R277 R278 R446 R466 R468
DEL TPJNC14 TPJNC16 JNC23
DEL Q15
DEL CN2
DEL U31

2015/01/07

- 01. P18 ADD C7101
- 02. P32 R393 R392 0402 change 0603
- 02. P50 ADD PR60 PR76 PR123

2015/01/21

- 01. P50 DEL PEC5

2015/01/26

- 01. P36 DEL EL4 EL5 EL6 EL7 EL8 EL10

2015/01/28

- 01. P34 ADD C170
- 02. P49 DEL PQ20

2015/01/29

- 01. P50 DEL PR75 PR76

1.0: 2015/03/11

- 01. P36 C564 Footprint 100UF_16V_SMD_H6 change C_B_3528
C572 Footprint 100UF_16V_SMD_H6 change C_B_3528

1.0: 2015/03/17

- 01. P19 ADD PR75 R391 PQ56 PC147

1.0: 2015/03/23

- 01. P9 ADD C673
- 02. P10 ADD C674

1.0: 2015/03/30

- 01. P32 ADD C675

1.0: 2015/04/07

- 01. P41 ADD R392